Name	**Dr. Sunil Jadav**	
Designation	**Assistant Professor**	
Date of Joining University	**Feb 2011**	
Qualification	**B.Tech (Electronics & Communication Engg.)** **M.Tech (VLSI Design & Automation)** **Ph.D (Semiconductor Devices)**	
Area of Specialization	**Semiconductor Device Modeling & Simulation** **Low Power IC Design, High Speed Interconnect Design** **Sensor Fabrication via Printed Electronics on Flexible substrates** **Students, who would like to purse Ph.D. internship or any research-oriented work with me, are always welcome.**	
Teaching Experience	**14.5 Years**	
Contact: E-mail / Phone	**+911292310141, +919540068364** **ymcavlsi@gmail.com, suniljadav@jcboseust.ac.in**	

EDUCATIONAL QUALFICATION:

Doctor of Philosophy, Electronics Engineering (VLSI Design)
YMCA University of Science & Technology, Faridabad, Haryana, Feb 2018.

- **Area of Research: Modeling & Simulation of Low Power VLSI Interconnects**

Master of Technology, VLSI Design & Automation, (2010)
Bachelor of Technology, Electronics & Communication Engineering, (2007)
National Institute of Technology, Hamirpur, Himachal Pradesh, India
(Institute of National Importance) 2010.

RESEARCH INTERESTS

Before joining YMCAUST, he has worked as Assistant Professor in Electronics & Communication Engineering Department of National Institute of Technology, Hamirpur. During his work in N.I.T Hamirpur, he has effectively utilized and worked on various VLSI EDA/CAD Tools/Semiconductor Process and on field programmable gate array

architecture development and low-power circuit design. He has published more than 40 papers in refereed journals and Conferences. His research interests include digital and analog IC design for low-power electronics, for portable computing, and High Speed Low power VLSI Interconnect. Another key interest in device and circuit level SPICE Simulation for modeling the behavior of semiconductor device and circuits.

One of his team is working on sensor design and fabrication on low cost flexible substrates. The research group is more focused on design and development of resistive sensor such as strain gauge, High sensitive Electrode designs for electrochemical applications or thin films.

AREAS OF TEACHING EXPERTISE

- Low Power VLSI Design
- VLSI interconnects
- CMOS Digital VLSI Design
- Analog IC design
- Printed Electronics
- Sensors and Signal conditioning
- Telemetry data processing and recording
- Electronics devices

PREVIOUS WORK /TEACHING EXPERIENCE

J.C.Bose University of Science & Technology, YMCA, Faridabad: 2011- Till date currently working as Assistant Professor in Electronics Engineering department.

National Institute of Technology, Hamirpur, HP: 2010-2011: Worked as Assistant Professor in ECE department. Worked and learned about various EDA and CAD Tool theoretical and simulative models.

Industrial Experience*:* 2007-2008, worked as Engineer in Electrical division for Nidan Packing Pvt. Limited.

AWARDS / DISTINCTIONS

- Received **Scholarship from Ministry of Human Resource Development, Govt. of India** in 1996 under "National Policy on Education-1986".
- Received PG **Scholarship from All India Council for Technical Education, Govt. of India** in 2008-2010 under "AICTE PG Scholarship Scheme".

- ❑ **Qualified GATE** exam in Electronics & Communication Engineering in 2006, conducted by **Indian Institute of Technology Kanpur, India.**
- ❑ **Certificate of Merit given by Hon'ble Vice-chancellor Dr. R. P. Bajpai** in year 2006 for representing the University in **North Zone All India Inter-University Tournament (Volley ball).**
- ❑ **Certificate of Excellence given by Director National Institute of Technology Hamipur, Himachal Pradesh for winners of Volley ball and Cricket Tournament** in year 2008-2009 organized by Sports Department of NIT.
- ❑ Paper Presentation award given by **VLSI Society of India** under theme **VLSI Interconnect" by C.P.Ravi kumar, Chairman, Texas Instruments India 2010.**
- ❑ **Certificate of Appreciation given by Prof. (Dr.) I.K Bhat, Director NIT Hamirpur** for conducting a Lab session during the workshop, 2010.
- ❑ **Research Award** for publication of research papers in SCI journal, Award given by **Hon'ble Vice-Chancellor Prof. (Dr.) Dinesh Kumar** for the year 2017, 2018.
- ❑ **Certificate of Appreciation given by Electronics Engineering Department** for organizing the workshop on VLSI Design- Mind to Market 2019
- ❑ **Selected and Registered as Translator in NPTEL Project of MHRD** managed by **Indian Institute of Technology Madras** Chennai India 2019.
- ❑ **Certificate of Appreciation** given by **Indian Institute of Science, Bangalore** for NPTEL work 2020.
- ❑ **Certificate of Commendation** given by **Hon'ble Vice-Chancellor Prof. (Dr.) Dinesh Kumar** for Translation of NPTEL modules 2020-2021.
- ❑ Received certificate of **Appreciation for Best Paper Award** in International Conference on Recent Developments in Electrical And Electronics Engineering, AICTE Sponsored by Dept. of Electrical Engineering JC Bose YMCA Faridabad.

PROFESSIONAL MEMBERSHIPS / ORGANIZATIONS

- ➢ Life Time Member of **Indian Society for Technical Education**
- ➢ Life Time Member of **Institution of Engineers**
- ➢ Life Time Member of **International Association of Engineers**
- ➢ Life Time Member of **Indian Science Congress Association**

COMMUNITY INVOLVEMENT / ADMINISTRATIVE ACTIVITY / SERVICES TO UNIVERSITY:

- **University B.Tech. admission committee core team** member (2011-2020)
- **Dept. M.Tech./Ph.D admission committee core team member** (2011-2020)

- **Training and Placement Coordinator (EE) (Training & Placement Office Cell)** (2013- Till date)
- **AICTE Co-Coordinator of the Dept. and core team member of the EOA**(extension of approvals) team (2015-2018)
- **Coordinator for In-plant Industrial Assessment of B.Tech students** (2015-2019)
- **Dept. Credit Base System** (CBS) Coordinator
- **Examination related work in affiliating Institutes** (Centre Supdt. Deputy Suptd.)
- Member of syllabus Committee
- Member of Student Council Election Core committee (2018-19)
- **University/Dept. Level Coordination committee member during NAAC and NBA visit**
- **Assistant Supdt. For the UGC-NET, AMIE Examination (Twice)**
- **Sessional Examination Coordinator** (During 2012-2014, 2017-2018)
- **Performing the duties of anti-ragging form last five years**
- Auditor for Library stock verification.
- **Coordinator at B.Tech and M.Tech Level course.**
- **Member of discipline committees in CULYMCA.**
- **Member of equal opportunity Cell.**
- **Member of Faculty of Engineering & Technology.**
- University foundation day celebration **contribution as corporate life**.
- **Organizing committee member** of National Conference on Role of Science and Technology Towards "Make in India" 5-7th March 2016
- **Organizing committee member** for Faculty Development Program on VLSI Design-Mind to Market 2019
- **Organizing committee member** for Faculty Development Program on VLSI Design-Mind to Market 2019
- **Organizing committee member** for Workshop on System Design Using IOT 2018
- **Contribution in National Integration:**
- Act as Presiding officer in Vidhansabha Election
- Act as a Zonal Magistrate in Loksabha Election
- Act as a Presiding Officer in Panchyat Election
- **Feedback Coordinator at Dept. Level:**
- Peer Group Feedback Coordinator
- Parent Feedback Coordinator
- Alumni Feedback Coordinator at Dept. Level
- Worked as organizing **Joint secretary/Member in International/National Conference** organized by JC Bose YMCA
- Worked for **Establishment Cell of the University**: Activities such as written test, scrutiny of applications for a recruitment process.
- **Inspecting officer For the UPSC (IAS pre)** Examination (Twice)
- Reviewer of various repute Journals

PUBLICATIONS / PRESENTATIONS / ABSTRACTS

Published Journals Papers (SCI/SCIE/Scopus/Web of Scienec):

1. N. Yadav, S. Jadav and G. Saini, **"Linearity Performance and Harmonic Distortion Analysis of Gate-over-Pockets Hetero-Dielectric Dual-Metal-Double-Gate TFET for RF Applications,"** has been published in Journal of **Micro and NanoStructures by Elsevier (SCI/SCIE) (Impact Factor: 3.1) (2025)**
2. Sunil Jadav "Estimation of bandwidth, voltage swing and DC coefficients for VLSI interconnects: current mode technique" **has been published in International Journal of Electronics Letters, published by Taylor and Francis. (SCI/SCIE) (Cite Score: 1.8), 2024.**
3. Nisha Yadav, Sunil Jadav, Gaurav Saini "**Steep sub-threshold swing Double - Gate tunnel FET using source pocket engineering: Design guidelines" has been published in** Micro and Nanostructures**, published by Elsevier (SCI/SCIE) (Impact Factor: 3.1), 2024.**
4. Malik, A., Jadav, S. & Gupta, S. **A multilevel qubit encryption mechanism using SHA-512. Multimed Tools Appl (2023).** https://doi.org/10.1007/s11042-023-16613-1
5. Shweta, Sunil Jadav, Rohit Triphathi "A Review on CO based Flexibile Sensor " **has been published in International Journal titled as "Sensor Review" published by Emeralad Group. (SCI/SCIE) (Impact Factor : 1.670), April 2023.**
6. Kuldeep Singh, Sunil Jadav, Shubham Tayal, Lalit Rai, Preet Kaur, Rajneesh Sharma "Power Efficient Vedic Multiplier " **has been published in International Journal of Electronics , published by Taylor and Francis. (SCI/SCIE) (Impact Factor : 1.670), Jan 2023.**
7. Nisha Yadav, Sunil Jadav, Gaurav Saini "Impact of Gate Length and Doping Variation on the DC and Analog/RF Performance of sub - 3*nm* Stacked Si Gate-All-Around

Nanosheet FET" **has been published in Silicon journal , published by Springer (SCI/SCIE) (Impact Factor : 2.670), July 2022.**

8. Nisha Yadav, Sunil Jadav, Gaurav Saini "Geometrical Variability Impact on the Performance of Sub-3nm Gate-All-Around Stacked nanosheet FET" **has been published in Silicon journal , published by Springer (SCI/SCIE) (Impact Factor : 2.670), March 2022.**
9. Sunil Jadav, Shubham Tayal "Gate stack Optimization of a vertically stacked nanosheet FET for digital/Analog/RF applications" **has been published for in journal of Computational Electronics, published by Springer (SCI/SCIE) (Impact Factor : 1.807), March 2022.**
10. Anjali Malik Sunil Jadav Shailender Gupta "Assessment of diverse image encryption mechanisms under prevalent invasion" **has been published in Multimedia Tools and Applications, published by Springer (SCI/SCIE) (Impact Factor : 2.757), 2021.**
11. Sunil Jadav, Rajeevan Chandel Munish Vashishath "High speed RLC equivalent RC delay model using normalized asymptotic function for global VLSI interconnects" **has been published in Microelectronics Journal (2020) Elsevier, Vol. No 107, (SCI/SCIE) (Impact Factor : 1.67).**
12. Sunil Jadav, Rajeevan Chandel "High performance 9T adiabatic SRAM and novel stability characterization using pole zero placement" has been published in **Analog Integr Circ Sig Process (2018) springer (SCI/SCIE/Scopus/UGC Approved) (Impact Factor : 1.337).**
13. Sunil Jadav, Munish Vashishath, Rajeevan Chandel "High speed RLC equivalent RC delay model for global VLSI interconnects" has been published in **Analog Integrated Circuit Signal Processing (2018) springer (SCI/SCIE/Scopus/UGC Approved) (Impact Factor : 1.337).**
14. **Sunil Jadav**, Garima Jain "Monte Carlo Analysis of Inductor-less Wideband Amplifier" has been published in **Journal of Information and Optimization**

Sciences (**Taylor & Francis**), pp 781-789, Vol. 38, 2017. **(UGC Approved/ ESCI/ Web of Science)**

15. Sunil Jadav, Munish Vashishath, Rajeevan Chandel "**RLC equivalent RC delay model for global VLSI interconnect in current mode signaling**, has been published in International Journal of Modeling & Simulation **(Taylor-Francis)** Vol. 35 Issue 1, 2015. **(UGC Approved/Scopus/ISI/).**
16. Sunil Jadav, Munish Vashishath, Rajeevan Chandel "**Modeling the Impact of Fundamental and Quantum Resistance on the Performance of SWCNT Based RLC Interconnects**, has been published in **International Journal of Modeling: Electronics Networks Devices and Field**. **(SCI/SCIE/UGC Approved/Scopus/ISI) (Impact factor: 1.296)**
17. Shubham Tayal, Ashutosh Nandi, Shikhar Gupta, Sunil Jadav "**Study of Inner-Gate Engineering Effect on Analog/RF Performance of Conventional Si-Nanotube FET"** has been accepted for Publication in Journal of **Journal of Nanoelectronics and Optoelectronics. (SCIE/Scoups/UGC Approved) Impact Factor: 1.069)**

18. Sunil Jadav, Shubham Tayal "**Temperature Sensitivity Analysis of Inner-Gate Engineered JL-SiNT-FET: An Analog/RF Prospective**" has been published in **Journal of Cryogenics Elsevier** Vol. 18, pp. No. 1-6 , 2020. **(SCI/UGC Approved/ Scopus) (Impact Factor: 2.226).**

19. Sunil Jadav, Munish Vashishath, Rajeevan Chandel "**A Superior Delay Estimation Model for VLSI Interconnect in Current Mode Signaling**, has been published in **World Academy of Science Engineering & Technology (France)** Vol. 9 , No 2, 2015. **(UGC Approved/Scopus/ISI)**

20. Sunil Jadav, Munish Vashishath, Rajeevan Chandel "**Carbon Nanotube Based Delay Model For High Speed Energy Efficient on Chip Data Transmission Using: Current Mode Technique**" has been published in International Journal of Electrical & Electronics Engineering by **Wireilla Scientific Publications (New South Wales, Australia)**, Vol. 3 No. 4, 2014. **(UGC Approved)**

21. Sunil Jadav, Shubham Tayal "Power-Delay Trade-Offs in Complementary Metal-Oxide Semiconductor Circuits Using Self and Optimum Bulk Control" has been published in **Sensor Letter Journal of American scientific Publisher Vol**. 18, pp. 210-215, No. 3 , 2020. **(UGC Approved/ Scopus)**

22. **Sunil Jadav**, Gargi Khanna, and Ashok Kumar, "**High Speed Energy Efficient signal Transmission on Global VLSI Interconnect**," has been published in **International Journal of Information and Telecommunication Technology**, pp. No- 52 -56 on Nov. 06, 2010

23. **Sunil Jadav**, Puneet Goyal, Munish Vashistha, Rajeevan Chandel "**Study and Performance Analysis of Two Stage High Speed Operational Amplifier Using Indirect Compensation**", has been published in **International Journal Engineering Science and Technology**, ISSN: 2250-3498, Vol.2, No. 4, August 2012, pp. No- 840-846.
24. Puneet Goyal **Sunil Jadav** Munish Vashishath, Abhishek "**Study and Performance Analysis of High Frequency and High Speed Operational Amplifier**"has been published in **International Journal of Electronics Communication and Computer Engineerin**g, Vol. 4, No. 2, 2013.

25. **Sunil Jadav**, Munish Vashistah "**Design and Validation of threshold Model Using BSIM3v 3.2.2** "has been published in **International Journal of Advanced Research in Electrical Electronics and Instrumentation Engineering**, Vol. 2, No. 10, oct 2013.

26. Nisha Yadav, Sunil Jadav "**Efficient Energy Recovery in 9T Adiabatic SRAM Cell Using Body Bias**" has published in **International Journal of VLSI & Embedded System**, Vol. 5, March 2014.

27. Shubham Tayal, Sunil Jadav, Munish Vashishath "**Implementation of Logic Gates Using Charge Recycling MTCMOS Technology**" has been published in **International Journal of VLSI & Embedded System**, Vol. 2, May 2014.

28. Sunil Jadav, Munish Vashishath, Rajeevan Chandel "**Current Mode signalling for Global VLSI interconnect:-A Review**" has been published in **YMCAUST Journal of Research**, Vol. 2, Issue 1, Jan 2014.

29. Sunil Jadav Munish Vashishath, Rajeeevan Chandel, Vikrant "**Design And Performance Analysis Of Ultra Low Power 6t SRAM Using Adiabatic Technique**" has been published in International Journal of VLSI &Communication Systems, pp 95-105, Vol.3, No. 3, 2012.

List of International Conference Publications/ Attended

30. Jadav Sunil Vashishath Munish Chandel Rajeevan **"A Novel Delay Model for Step Analysis and Bandwidth Estimation of VLSI Interconnect for Current Mode Signaling"** has been presented in international conference on **recent trends in engineering and material sciences, pp -12, 17-19 March 2016**

31. Sunil Jadav, Gaurav Saini, Pankaj Kr.Pal, Ashwani Rana, "**Leakage Behavior of Under Lap Finfet Structure**: A simulation Study," has been published in IEEE proceeding of ICCCT'10, pp. No- 302-305, Sept, 2010.
32. Sunil Jadav, Ashok Kumar, and Gargi Khanna, "**Low Power High Throughput Current Mode Signalling Technique for Global VLSI Interconnect**," has been published in IEEE proceeding of ICCCT'10, pp. No- 290-295, Sept, 2010.
33. Sunil Jadav, Munish Vashishath, Rajeevan Chandel "**Close form delay model for on chip 9ignaling with resistive load termination using: Current mode technique**, in (ICIIS), pp. 1-6 Gwalior,India 2014. (IEEE Explore)
34. Sunil Jadav, Atul Kumar Maurya, , Gagnesh Kumar, Devendra Giri "**Performance Analysis of Various Adiabatic Logic Circuits**," has been published in International Conference on Advances in Computing & Communication proceeding of ICACC'11 (IEEE-MTTS), pp. No- 407-410, April, 2011.
35. S. Jadav, A. K. Nishad, R. Chandel, D. Solanki "**Gate Diffusion Input: A Power Efficient Design Technique for VLSI Circuits**," has been published in International Conference on Advances in Computing & Communication proceeding of ICACC'11 (IEEE-MTTS), pp. No- 432-435, April, 2011.

36. Sunil Jadav, Gargi Khanna, and Ashok Kumar, "**Analysis of Current mode Drivers for VLSI Interconnect System**," has been published in Proc. 14th IEEE/VSI VLSI Design and Test Symposium, Organized by the VLSI Society of India, on July 7-9, 2010.
37. Nisha Goyal, Sunil jadav, Vikrant, Sandeep Kaushal, Khushboo "**Leakage Control in Logic Gates Using Optimum Body Bias**" has been published in International Conference on VLSI, MEMS & NEMS, 2012.
38. Nisha Yadav, Sunil jadav, Gaurav Saini "**DC/Analog RF Performance Analysis of Multi-Bridge Channel FET with Variation in Gate Work Function**" has been published in International Conference on Advancement in Technology, 2022.
39. Malik, A., Jadav, S., Gupta, S. (2023). A Multilevel Secured Mechanism for Data Protection. In: Singhal, P., Kalra, S., Singh, B., Bansal, R.C. (eds) Recent Developments in Electrical and Electronics Engineering. **Lecture Notes in Electrical Engineering, vol 979. Springer, Singapore.** https://doi.org/10.1007/978-981-19-7993-4_16. **(Scopus), April 2023.**
40. Nisha Yadav, S. Jadav and Gaurav Saini, "A revie on Role Epitaxial Engineering in improving the Drive Current and Subthreshold Swing in Area Scaled Tunnel FETs," *has been published in* ***International Conference on Computer Electronics and Electrical Engineering and their application (IC2E3-2023)*****,** NIT Uttrakhand, India, 2023, **(Scopus), June 2023.**
41. Shweta, S. Jadav and R. Tripathi, "Criterion for Capacitive Interdigitated Electrode for Gas Sensing Applications," *2023* ***International Conference for Advancement in Technology (ICONAT)*****,** Goa, India, 2023, pp. 1-4, doi: 10.1109/ICONAT57137.2023.10080414. **(Scopus), April 2023.**
42. Shweta, Sunil Jadav "Modelling the Impact of Grain Size on carrier concentration & Sensitivity for Gas sensing Applications" **has been published in 2nd International Conference on Computer, Electronics, Electrical Engineering and their Applications(IC2E3 2024) organised by NIT Uttrakhand, India (IEEE).**

43. Malik, A., Jadav, S. & Gupta, S. Paper titled **"A secured multilevel data protection mechanism"** published in International Conference on Research and innovation for Sustainable Development (ICRISD-2024), organized by MDU Rohtak, Haryana, India

National Conference

44. Sunil Jadav Munish Vashishath Rajeevan Chandel "**Sub-threshold Leakage Reduction of 6T SRAM Cell Using Optimum Bulk Bias**, has been published in National Conference on Recent Development in Electronics, Jan. 2013.
45. Paper Published on "**Graphene-Promising Candidate of Nanoelectronics**" in "**RAEEE-09**" December 23-24 ,2009 ,**National Conference on Recent Advances in Electrical & Electronics Engineering** ,Organized by Department of Electrical Engineering **National Institute of Technology Hamirpur**, pp. 529-533.
46. Paper Published on "**Recent Advances in High Resolution Lithography for VLSI Application**" in "**ETCC-08**" December 30-31 ,2008 ,**National Conference on Emerging Trends in Computing and Communication** ,Organized by Department of Computer Science **National Institute of Technology Hamirpur**, pp. 363-368.
47. Paper Published on "**Source Follower Based Track-and-Hold Circuit for High Speed Wireless Communication**" in "**ETIC-2010**" march 27 ,2010 ,**National Conference on Emerging Trends in IT and Computing**, Organized by Department of IT/MCA **Gurgaon Institute of Technology & Management**, Gurgaon (Haryana), pp. 26-29.
48. Paper Published on "**Analysis of Wideband Amplifier with Different Load Condition**" in "**ETIC-2010**" march 27 ,2010 ,**National Conference on Emerging Trends in IT and Computing**, Organized by Department of IT/MCA **Gurgaon Institute of Technology & Management**, Gurgaon (Haryana), pp. 184-186

49. Paper Published on "**Low Power Track-and-Hold Circuit for Wideband Acquisition System in 0.18um CMOS Technology**" in "**NCWCVD-2010**" march 27-28, 2010 ,**National Conference on Wireless Communication & VLSI Design**, Organized by Department of Electronics & Comm., Technically Supported By: **IEEE (MP SS) Gwalior Engineering College,** Gwalior (M.P)
50. Paper Published on "**Carbon Nanotubes & its Application for VLSI Interconnects in Wireless Comm.**" In "**E-Manthan-2010**" April 02-03 ,2010 ,**National Conference on Electronics Comm. & Instrumentation Collaboration with IETE**,

Organized by Department of Electronics & Comm. **College of Science & Engineering,** Jhansi (U.P), pp. 159-162

51. Paper Published on "**Chanel Width Tapering to Reduce the Delay and Power Dissipation in Domino CMOS Circuits** " in "**E-Manthan-2010**" April 02-03 ,2010 ,**National Conference on Electronics Comm. & Instrumentation Collaboration with IETE**, Organized by Department of Electronics & Comm. **College of Science & Engineering,** Jhansi (U.P), pp. 313-316
52. Paper Published on "**Low Power Ultra Wideband Amplifier for Wireless Application**" , in "**E-Manthan-2010**" April 02-03 ,2010 ,**National Conference on Electronics Comm. & Instrumentation Collaboration with IETE**, Organized by Department of Electronics & Comm. **College of Science & Engineering,** Jhansi (U.P), pp. 107-110.
53. Paper Published on "**Study and Comparsion with CNTFET with Conventional MOSFET**" , in "**RSTTMI-2016**" March 05-07 ,2016 ,**National Conference on Role of Science & Technology Towards "Make In India"**, Organized by Department of YMCA University of Science & Technology Faridabad, pp. 295-299, ISBN:978-93-5265-4413.
54. Paper Published on "**Nanowire: A Future Interconnect**" , in "**RSTTMI-2016**" March 05-07 ,2016 ,**National Conference on Role of Science & Technology Towards "Make In India"**, Organized by Department of YMCA University of Science & Technology Faridabad, pp. 315-318, ISBN:978-93-5265-4413.
55. Paper Published on "**Process Investigation for a Junction Diode**" , in "**RSTTMI-2016**" March 05-07 ,2016 ,**National Conference on Role of Science & Technology Towards "Make In India"**, Organized by Department of YMCA University of Science & Technology Faridabad, pp. 319-321, ISBN:978-93-5265-4413.
56. Paper Published on "**Power efficient 1 bit comparator**" , in "" March 05-07 ,2016 ,**National Conference on VLSI AND SIGNAL PROCESSING"**, Organized by Department of ECE NIT Hamirpur Himachal Pradesh, 2014.

List of Book Chapters Authored/Edited:

1. Nisha Yadav Sunil Jadav chapter Titled as **"Simulation and Analysis of Gate Stack DG MOSFET with Application of High-k Dielectric Using Visual TCAD"** published by CRC Press in book title **High-k Materials in Multi-Gate FET Devices.**
2. **Sunil Jadav Edited/Translated book Titled as "Op-Amp Practical Applications: Design, Simulation and Implementation" published by NPTEL. Link:swayam.gov.in/NPTEL.**
3. N. Yadav, S. Jadav and G. Saini, **"The Tunnel FET: Fundamentals, Calibration and Simulation"** in ***Next-Generation Nanotechnology: Design and Techniques for Ultra-Nanoscale Applications***, Wiley-Scrivener, 2024, Chapter ID-11.
4. Sunil Jadav **"High Performance SBT Multipliers for Computing Applications"** in ***High-Performance Automation Methods for Computational Intelligent Systems: Challenges, Opportunities, and Applications"***, **which will be published by CRC Press (Taylor & Francis Group) 2024**, Chapter No. 3.

Ph.D Student under Supervision:

Sr.No.	Name of Candidate	Research Topic
01	Nisha Yadav	**Design and Analysis of Steep sub-threshold devices for futuristic electronics**
02	Shweta	**Analysis and Design of efficient Flexible Gas sensor**
03	Anjali Malik	**Analysis and Design of Secured mechanism for Data Communication**

List of Patents:

1. **N. Yadav,** S. Jadav and G. Saini (2024). ***A Gate-over-pockets Hetero-dielectric Dual-metal Double-gate Tunnel Field-effect Transistor for Steep Switching***, Indian Patent, AFR No. 202411065126.
2. **S. Jadav,** Rakhi, D.Shukla, L. Rai (2024). ***Design and Fabrication of Electronic Low Pass Filter On Paper Substrate,*** Indian Patent, AFR no.: 202411012668 A, the Patent Office Journal No. 09/2024 Dated 01/03/2024.

M.Tech Students Research Guidance status

Sr.No	M.Tech Degree	Enrolment Number	Thesis Submitted	Degree Awarded
1	Sandeep Kaushal	MVLSI-262-2k10	N/A	yes
2	Nisha Goyal	MVLSI-269-2K10	N/A	yes
3	Puneet Goyal	MVLSI-261-2K10	N/A	yes
4	Ravinder Singh pokharia	MVLSI-911-2k11	N/A	yes
5	Shubham Tayal	MVLSI-155-2K12	N/A	yes
6	Nisha Yadav	MVLSI-150-2K12	N/A	yes
7	Meenu Rani	MVLSI-347-2K13	N/A	yes
8	Garima Jain	MVLSI-545-2K14	N/A	yes
9	Sanjeet Dahyia	MVLSI-553-2K14	N/A	yes
10	Pooja Rathi	MVLSI-552-2K14	N/A	yes
11	Subhanshu kr. Verma	MVLSI-914-2k11	N/A	yes

12	Akhil Daulta	MVLSI-900-2K11	N/A	yes
13	Himanshi Aggarwal	MVLSI-904-2k16	N/A	yes
14	Aishwarya Singh	MVSLI-902-2k16	N/A	yes
15	Vishant Malik	MVLSI-916-2k16	N/A	yes
16	Vikrant	MVLSI-266-2k10	N/A	yes
17	Himani		N/A	Yes
18	Kuldeep Choudhary		N/A	Yes
19	Rakhi Chandila			Yes
20	Mohit 2021-2023			Yes
21	Rishab Kaushik	2023-2024	NO	yes

Training Courses

Sr.No	Programs STC/FDP	Duration with Date	Organized by	
1	Workshop on Nanotechnology & Embedded Systems	23rd July-3rd August 12	YMCAUST	Two Week
2	Entrepreneurship	8th Jan-22nd Jan13	UIET KUK	Two week
3	Embedded Systems & Hardware Description Language	20th May-24th May13	NIT Hamirpur	One Week
4	Emerging materials: Characterization and Applications	June 13-17, 2014	NIT KuK	One Week
5	Synthesis and Characterization Techniques of Smart materials	Sept 22-26, 2014	NIT KUK	One week
6	Matlab and Simulink	11th -16th Feb2015	YMCAUST	One week

7	New trends in Electronics & Communication	17th -21st Aug 2015	YMCAUST	One Week
8	Effective Teaching	Jan 18-22, 2016	NITTTR,CHD	One week
9	CMOS Mixed Signal and Radio Frequency VLSI Design	26th Dec-4th Feb 2017	IIT Kharagpur	Two Week
10	Real Time Data Acquisition and Analysis using Lab VIEW	May 8-12, 2017	YMCAUST	One week
11	System Design Using IOT 2018	6th -8th march 2018	YMCAUST	Three day worksh op
12	Skill Development Course On Semiconductor Device Fabrication and Characterization	8th Aug-14th Aug 2018	CEERI PILANI, RAJ.	7 days
13	Workshop on VLSI Design-Mind to Market 2019	28th Jan-2nd Feb2019	YMCAUST	One week
14	Digital and Analog VLSI Design	13th Sept to 17 Sept 2021	NITTTR CHD	One Week
15	Recent Challenges and Developments in Solar Energy Technologies and Its Applications	24/01/2022 to 29/01/2022	YMCAUST	One week
16	Cloud Computing and Internet of Things	07/02/2022 to 12/02/2022	YMCAUST	One week
17	Work life balance for technocrats	20/5/2022 to 24/5/2022	YMCAUST	One week

18	VLSI Design and Nano-electronics: Emerging Challenges & Opportunities	Sept 01-08, 2022	IIIT JABALPUR	ONE WEEK
19	Sustainable Environmental Management	20/02/2023 to 24/02/2023	NiTTTR Chd	One Week
20	CMOS VLSI Design	MOOC 2023	IIT Roorkee	Eight Week

List of Certificate Courses Completed from NPTEL/Swayam:

1. Completed a certificate course on "**Advanced Composite material Manufacturing Process**" by Indian Institute of Technology Mandi, HP India, Feb 2021.
2. Completed a MOOC course on "**CMOS VLSI Design**" from NPTEL Swayam Portal conducted by Prof. Sudeb Dasgupta from IIT Roorkee India, Jan 2021
3. Completed a course on **Digital Transformation in Teaching Learning Process (DTITLP)** course organized by NPIU, and conducted by IIT Bombay on SWAYAM, April 2020.
4. Completed a course on **Digital Transformation in Teaching Learning Process (DTITLP)** course organized by NPIU, and conducted by IIT Bombay on SWAYAM, Feb-March 2020.
5. Completed a MOOC course on "**CMOS VLSI Design**" from NPTEL Swayam Portal conducted by Prof. Sudeb Dasgupta from IIT Roorkee India, Jan 2023.