SCHEME & SYLLABUS

for

M.TECH. COURSE

in

VLSI DESIGN

(w.e.f. Session 2026-2027)

DEPARTMENT OF ELECTRONICS ENGINEERING

J. C. BOSE UNIVERSITY OF SCIENCE AND TECHNOLOGY, YMCA, FARIDABAD

J. C. BOSE UNIVERSITY OF SCIENCE & TECHNOLOGY, YMCA, FARIDABAD

VISION

J. C. Bose University of Science & Technology, YMCA, Faridabad (erstwhile YMCA University of Science and Technology) aspires to be a nationally and internationally acclaimed leader in technical and higher education in all spheres which transforms the life of students through integration of teaching, research and character building.

MISSION

- To contribute to the development of science and technology by synthesizing teaching, research and creative activities.
- To provide an enviable research environment and state-of-the-art technological exposure to its scholars.
- To develop human potential to its fullest extent and make them emerge as world class leaders in their professions and enthuse them towards their social responsibilities.

Department of Electronics Engineering

VISION

To be a Centre of Excellence for producing high-quality engineers and scientists capable of providing sustainable solutions to complex problems and promoting cost-effective indigenous technology in the area of Electronics, Communication & Control Engineering for Industry, Research Organizations, Academia and all sections of society.

MISSION

- To frame a well-balanced curriculum with an emphasis on basic theoretical knowledge as well the requirements of the industry.
- To motivate students to develop innovative solutions to the existing problems for betterment of the society.
- Collaboration with the industry, research establishments and other academic institutions to bolster the research and development activities.
- To provide infrastructure and financial support for culmination of novel ideas into useful prototypes.
- To promote research in emerging and interdisciplinary areas and act as a facilitator for knowledge generation and dissemination through Research, Institute - Industry and Institute-Institute interaction.

ABOUT THE DEPARTMENT

The Department of Electronics Engineering at J. C. Bose University of Science & Technology, YMCA, Faridabad (formerly YMCA University of Science & Technology, Faridabad) carries forward a distinguished legacy of technical education and industry-oriented learning. The University, established in 2009, evolved from the erstwhile YMCA Institute of Engineering, Faridabad, which was founded in 1969 as a joint venture between the Government of Haryana and the National Council of YMCA of India, with active support from overseas agencies of West Germany. The institution was established with the vision of developing highly skilled, practically oriented engineering professionals to meet the evolving technical manpower requirements of industry.

The Department of Electronics Engineering, established in 1969, has consistently contributed to academic excellence and technological advancement in electronics and allied domains. Since 1997, the Department has been offering undergraduate programmes leading to the B.Tech. degree in Electronics and Communication Engineering, Electronics Engineering (Specialization in Internet of Things), and Electronics and Computer Engineering, each of four years' duration. Admissions to the undergraduate programmes are conducted through centralized counselling as nominated by the State Government for first-year admissions, while admissions to the second year are offered through the lateral entry entrance process. In addition to undergraduate education, the Department offers postgraduate programmes leading to the M.Tech. degree in VLSI Design and Electronics & Communication Engineering. The Department also conducts Ph.D. programmes to promote advanced research and innovation in emerging areas of electronics and communication technologies.

All programmes offered by the Department are duly approved by AICTE and UGC and are designed to maintain strong academic standards while addressing contemporary industry requirements. The Department has established a strong reputation for producing competent engineering graduates with an excellent track record of student placements since its inception. To support quality teaching, learning, and research, the Department is equipped with robust academic infrastructure comprising 11 laboratories, 10 lecture halls, one conference room, and six workshops. The Department is supported by a dedicated and experienced faculty team consisting of 3 Professors, 6 Associate Professors, and 15 Assistant Professors. At present, 21 faculty members hold Ph.D. degrees across diverse areas of specialization, contributing significantly to teaching, research, consultancy, and academic development.

The curriculum of undergraduate and postgraduate programmes has been developed with active participation from industry to ensure relevance to current technological trends and professional requirements. The Department regularly organizes expert lectures and technical interactions with industry professionals each semester to strengthen the academic–industry interface. To enhance experiential learning and professional readiness, one semester of internship/training is mandatory for every B.Tech. student. Special emphasis is placed on project-based learning, laboratory practice, and workshop activities to promote innovation, problem-solving ability, and skill enhancement. The University follows a Choice Based Credit System (CBCS) and NEP, enabling students to pursue elective and audit courses according to their academic interests and career aspirations, thereby encouraging interdisciplinary learning and academic flexibility.

Program Educational Objectives (PEO):

Students of the Master of Technology programs in VLSI Design will demonstrate

1. To educate and train the graduates with knowledge and skills necessary to formulate, design and solve problems in Analog, Digital & Mixed Signal VLSI system design, VLSI Signal Processing, Real Time Embedded System design and Hardware Software Co-Design.
2. To provide technical skills in software and hardware tools related to the design and implementation of integrated Circuits, System on Chip for real-time applications.
3. To provide scope for Applied Research and innovation in the various fields of VLSI and Embedded Systems, and enabling the students to work in the emerging areas.
4. To enhance communication and soft skills of students to make them work effectively as a team

Program Outcomes (PO):

1. Ability to acquire and apply in-depth knowledge in the area of Electronics and Communication Engineering and contribute to the state-of-the-art.
2. An ability to independently carry out research /investigation and development work to solve practical problems
3. An ability to write and present a substantial technical report/document
4. An Ability to engage in life-long learning and learning through mistakes with/without external feedback.
5. An ability to understand the role of a leader, leadership principles and attitude conducive to effective professional practice of Electronics and Communication Engineering
6. An ability to understand the impact of research and responsibility to contribute to society.

GRADING SCHEME

Marks %	**Grade**	**Grade points**	**Category**
90-100	O	10	Outstanding
80 ≤ marks <90	A+	9	Excellent
70 ≤ marks < 80	A	8	Very good
60 ≤ marks < 70	B+	7	Good
50 ≤ marks < 60	B	6	Above average
45 ≤ marks < 50	C	5	Average
40 ≤ marks < 45	P	4	Pass
<40	F	0	Fail
	Ab	0	Absent

Percentage calculation= CGPA * 9.5

M. TECH. (VLSI Design)

Total Credits	**68**
Total Theory Subjects	**11+2 Audits**
Total Labs (including Projects)	**5**
Total Dissertation	**2**

SEMESTER-WISE SUMMARY OF THE PROGRAMME: M.TECH. (VLSI Design)

S.No.	Semester	No. of Contact Hours	Marks	Credits
1	**I**	**24**	**700**	**18**
2	**II**	**26**	**650**	**18**
3	**III**	**26**	**500**	**16**
4	**IV**	**32**	**500**	**16**
5	**MOOCs**	**-**	**-**	**6***
Total		**108**	**2350**	**74**

Note:

1. The scheme will be applicable from Academic Session 2019-20 onwards.
2. ***It is mandatory to pass the MOOC course(s) by all the students as per the implementation of credit transfer/ mobility policy of online courses of the University, as mentioned in Annexure-A at the end of the syllabus.**

Semester I

M. Tech. (VLSI Design)

Sr. No.	Category	Course Code	Course Title	Hours per week			Credits	Sessional Marks	Final Marks	Total
				L	T	P				
1	PCC	VDP-101-V1	RTL Simulation and Synthesis with PLDs	3	0	0	3	40	60	100
2	PCC	VDP-103-V1	Microcontrollers and Programmable Digital Signal Processors	3	0	0	3	40	60	100
3	PEC		Elective I	3	0	0	3	40	60	100
4	PEC		Elective II	3	0	0	3	40	60	100
5	PCC	VAC-301-V1	Research Methodology and IPR	2	0	0	2	40	60	100
6	AUD		Audit Course 1	2	0	0	0	40	60	100
7	PCC	VDP-105-V1	RTL Simulation and Synthesis with PLDs Lab	0	0	4	2	25	25	50
8	PCC	VDP-107-V1	Microcontrollers and Programmable Digital Signal Processors Lab	0	0	4	2	25	25	50
						Total	**18**	290	510	700

	Course	Course Title
Program Elective-I	**VDP-109-V1**	Physical Design Automation
	VDP-111-V1	Programming Languages for Embedded Software
	VDP-113-V1	Digital Signal and Image Processing
	VDP-115-V1	VLSI Technology with MEMS Applications
Program Elective-II	**VDP-117-V1**	Parallel Processing
	VDP-119-V1	System Design with Embedded Linux
	VDP-121-V1	CAD of Digital System
	VDP-123-V1	Device Modeling for Circuit Simulation

AUD	**AEC-301-V1**	English for Research Paper Writing
	VAC-302-V1	Disaster Management
	AEC-302-V1	Sanskrit for Technical Knowledge
	VAC-303-V1	Value Education
	VAC-112-V1	Constitution of India
	VAC-304-V1	Pedagogy Studies
	AEC-317-V1	Stress Management by Yoga
	AEC-304-V1	Personality Development through Life Enlightenment Skills.
	AEC-305-V1	Swami Vivekananda's thoughts

Semester II

M. Tech. (VLSI Design)

Sr. No.	Category	Course Code	Course Title	Hours per week			Credits	Sessional Marks	Final Marks	Total
				L	T	P				
1	PCC	VDP-102-V1	Analog and Digital CMOS VLSI Design	3	0	0	3	40	60	100
2	PCC	VDP-104-V1	VLSI Design Verification and Testing	3	0	0	3	40	60	100
3	PEC		Elective III	3	0	0	3	40	60	100
4	PEC		Elective IV	3	0	0	3	40	60	100
5	AUD2		Audit Course 2	2	0	0	0	40	60	100
6	PCC	VDP-106-V1	Analog and Digital CMOS VLSI Design Lab	0	0	4	2	25	25	50
7	PCC	VDP-108-V1	VLSI Design Verification and Testing Lab	0	0	4	2	25	25	50
8	PCC	VDP-110-V1	Minor Project	0	0	4	2	25	25	50
			Total Credits				**18**	275	375	650

	Course Name	Course Title
Program Elective-III	**VDP-112-V1**	Memory Technologies
	VDP-114-V1	SoC Design
	VDP-116-V1	Low power VLSI Design
	VDP-118-V1	CMOS RF Circuit Design
Program Elective-IV	**VDP-120-V1**	Communication Buses and Interfaces
	VDP-122-V1	Network Security and Cryptography
	VDP-124-V1	VLSI Signal Processing
	VDP-126-V1	ASIC's & FPGA

AUD 2 (Audit 2 should be different from audit 1)	**AEC-301-V1**	English for Research Paper Writing
	VAC-302-V1	Disaster Management
	AEC-302-V1	Sanskrit for Technical Knowledge
	VAC-303-V1	Value Education
	VAC-112-V1	Constitution of India
	VAC-304-V1	Pedagogy Studies
	AEC-317-V1	Stress Management by Yoga
	AEC-304-V1	Personality Development through Life Enlightenment Skills.
	AEC-305-V1	Swami Vivekananda's thoughts

VDP-101-V1 **RTL Simulation and Synthesis with PLDs**

L T P	CR		
3 0 0	3	Theory	60
		Class Work	40
		Total	100
		Duration of Exam	3 Hrs.

Course Objectives:

- To learn the basic of RTL programming.
- To learn the design entry by Verilog & VHDL.
- To learn the basics of ASIC, FPGA and SOC.
- To introduce the different design techniques of low power, RTL source code and soft IP.

Syllabus Contents:

Unit1: Introduction to HDLs, Top-down approach to design, Design of FSMs (Synchronous and asynchronous), Static Timing analysis, Metastability, Clock issues, Need and design strategies for multi-clock domain designs.

Unit 2: Design entry by Verilog/ VHDL/ FSM, Introduction to Verilog AMS.

Unit 3: Programmable Logic Devices, Introduction to ASIC Design Flow, FPGA, SoC, Floor planning, Placement, Clock tree synthesis, Routing, Physical verification, Power analysis, ESD protection.

Unit 4: Design for performance, low-power VLSI design techniques. Design for testability.

Unit 5: IP and Prototyping: IP in various forms: RTL Source code, Encrypted Source code, Soft IP, Netlist, Physical IP; use of external hard IP during prototyping

Unit 6: Case studies and Speed issues.

Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- Understand the basics of RTL programming.
- Design entries by using VHDL/ Verilog.
- Understand the basics of ASIC, FPGA & SOL.

Understand different design techniques for low-power RTL codes and soft IP.

References:

- Richard S. Sandige, “Modern Digital Design”, MGH, International Editions.
- Donald D Givone, “Digital principles and Design”, TMH
- Charles Roth, Jr. and Lizy K John, “Digital System Design using VHDL”, Cengage Learning.
- Samir Palnitkar, “Verilog HDL, a guide to digital design and synthesis”, Prentice Hall.
- Doug Amos, Austin Lesea, Rene Richter, “FPGA based prototyping methodology
- manual”, Xilinx
- Bob Zeidman, “Designing with FPGAs & CPLDs”, CMP Books

VDP-103-V1 **Microcontrollers and Programmable Digital Signal Processors**

L T P	CR		
3 0 0	3	Theory	60
		Class Work	40
		Total	100
		Duration of Exam	3 Hrs.

Course Objectives:

- To know programming model of ARM and learn instructions of ARM.
- To learn about interrupt, timer, memory and peripherals of ARM.
- To know about DSP architecture and learn programming.
- To learn application development of DSP.

Syllabus Contents:

Unit 1: ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces

Unit 2: Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.

Unit 3: LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT

Unit 4: Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family

Unit 5: VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations

Unit 6: Code Composer Studio for application development for digital signal processing, On chip peripherals, Processor benchmarking

References:

1. Joseph Yiu, “The definitive guide to ARM Cortex-M3”, Elsevier, 2nd Edition
2. Venkatramani B. and Bhaskar M. “Digital Signal Processors: Architecture, Programming and Applications” , TMH , 2nd Edition
3. Sloss Andrew N, Symes Dominic, Wright Chris, “ARM System Developer's Guide: Designing and Optimizing”, Morgan Kaufman Publication
4. Steve furber, “ARM System-on-Chip Architecture”, Pearson Education
5. Frank Vahid and Tony Givargis, “Embedded System Design”, Wiley
6. Technical references and user manuals on www.arm.com, NXP Semiconductor www.nxp.com and Texas Instruments www.ti.com

Course outcome:

At the end of this course, students will be able to

- Compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
- Identify and characterize architecture of Programmable DSP Processors
- Develop small applications by utilizing the ARM processor core and DSP processor based platform.

VDP-109-V1 **Physical Design Automation**

L T P	CR		
3 0 0	3	Theory	60
		Class Work	40
		Total	100
		Duration of Exam	3 Hrs.

Course Objectives:

- To introduce the physical design issues for VLSI automation.
- To familiarize performance issues of VLSI circuits, various delay models & its estimation.
- To introduce the placement & routing algorithms.
- To familiarize the concept of field programmable gate arrays, its design flow & its applications in various areas.

Syllabus Contents:

Unit 1: Introduction to VLSI Physical Design Automation.

Unit 2: Standard cell, Performance issues in circuit layout, delay models Layout styles.

Unit 3: Discrete methods in global placement.

Unit 4: Timing-driven placement. Global Routing Via Minimization.

Unit 5: Over the Cell Routing - Single layer and two-layer routing, Clock and Power Routing.

Unit 6: Compaction, algorithms, Physical Design Automation of FPGAs.

References:

- William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition.
- Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communication in a Public World", Prentice Hall, 2nd Edition
- Christopher M. King, ErtemOsmanoglu, Curtis Dalton, "Security Architecture, Design Deployment and Operations", RSA Pres,
- Stephen Northcutt, LenyZeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "Inside Network Perimeter Security", Pearson Education, 2nd Edition
- Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident Detection and Response", William Pollock Publisher, 2013.

Course Outcomes:

At the end of the course, students will be able to:

- Study automation process for VLSI System design.
- Understanding of fundamentals for various physical design CAD tools.
- Develop and enhance the existing algorithms and computational techniques for physical design process of VLSI systems.

VDP-111-V1 **Programming Languages for Embedded Software**

L T P	CR		
3 0 0	3	Theory	60
		Class Work	40
		Total	100
		Duration of Exam	3 Hrs.

Course Objectives:

1. To introduce the 'C' programming language for handling different hardware.
2. To introduce the OOP language.
3. To introduce the CPP programming language for controlling hardware.
4. To introduce scripting languages for handling data patterns.

Syllabus Contents:

Unit 1: Embedded 'C' Programming

- Bitwise operations, Dynamic memory allocation, OS services
- Linked stack and queue, Sparse matrices, Binary tree
- Interrupt handling in C, Code optimization issues
- Writing LCD drives, LED drivers, Drivers for serial port communication
- Embedded Software Development Cycle and Methods (Waterfall, Agile)

Unit 2: Object Oriented Programming: Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism

Unit 3: CPP Programming: 'cin', 'cout', formatting and I/O manipulators, new and delete operators, defining a class, data members and methods, 'this' pointer, constructors, destructors, friend function, dynamic memory allocation

Unit 4: Overloading and Inheritance: Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual functions

Unit 5: Templates: Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch- throw, Multiple Exceptions.

Unit 6: Scripting Languages: Overview of Scripting Languages – PERL, CGI, VB Script, JavaScript. PERL: Operators, Statements, Pattern Matching, etc. Data Structures, Modules, Objects, Tied Variables, Inter-process Communication, Threads, Compilation & Line Interfacing.

References:

- Michael J. Pont, "Embedded C", Pearson Education, 2nd Edition, 2008
- Randal L. Schwartz, "Learning Perl", O'Reilly Publications, 6th Edition, 2011
- A. Michael Berman, "Data structures via C++", Oxford University Press, 2002
- Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company, 1999
- Abraham Silberschatz, Peter B, Greg Gagne, "Operating System Concepts", John Wiley & Sons, 2005

Course outcome:

At the end of this course, students will be able to

- Write an embedded C application of moderate complexity.
- Develop and analyze algorithms in C++.
- Differentiate interpreted languages from compiled languages.

VDP-113-V1 **Digital Signal and Image Processing**

L T P	CR		
3 0 0	3	Theory	60
		Class Work	40
		Total	100
		Duration of Exam	3 Hrs.

Course Objectives:

- To introduce/review discrete time signals & systems.
- To explain FIR & IIR with design of structure.
- To introduce the design & implement filters using fixed point arithmetic.
- To introduce the image acquisition.
- To introduce color image processing

Syllabus Contents:

Unit 1: Review of Discrete Time signals and systems, Characterization in time and Z and Fourier domain, Fast Fourier Transform algorithms – In-place computations, Butterfly computations, bit reversals.

Unit 2: Digital Filter design: FIR - Windowing and Frequency Sampling, IIR – Impulse invariance, bilinear Transformation.

Unit 3: Fixed point implementation of filters – challenges and techniques.

Unit 4: Digital Image Acquisition, Enhancement, Restoration. Digital Image Coding and Compression – JPEG and JPEG 2000.

Unit 5: Color Image processing – Handling multiple planes, computational challenges.

Unit 6: VLSI architectures for implementation of Image Processing algorithms, Pipelining

References:

- J.G. Proakis, Manolakis "Digital Signal Processing", Pearson, 4th Edition
- Gonzalez and Woods, "Digital Image Processing", PHI, 3rd Edition
- S. K. Mitra. "Digital Signal Processing – A Computer based Approach", TMH, 3rd Edition, 2006
- A. K. Jain, "Fundamentals of Digital Image Processing", Prentice Hall
- Keshab Parhi, "VLSI Digital Signal Processing Systems – Design and Implementation", Wiley India

Course Outcomes:

At the end of this course, students will be able to

- Analyze discrete-time signals and systems in various domains
- Design and implement filters using fixed point arithmetic targeted for embedded platforms
- Compare algorithmic and computational complexities in processing and coding digital images.

VDP-115-V1 **VLSI Technology with MEMS Application**

L T P	CR		
3 0 0	3	Theory	60
		Class Work	40
		Total	100
		Duration of Exam	3 Hrs.

Course Objectives:

1. To introduce the students to the concept of molecular reorganization and the fundamentals of surfaces and interfaces
2. To introduce the students to the principles of different types of materials
3. To introduce the students to the concept of MEMS design and fabrication technology
4. To introduce the students to the different types of MEMS and their applications

Syllabus Contents:

Unit 1: Crystal growth: Wafer preparation, Processing considerations, Chemical cleaning, getting the thermal stress factors, etc. Epitaxy: Vapor-phase epitaxy basic transport processes & reaction kinetics, Doping & auto-doping, equipment, & Safety considerations, buried layers, Epitaxial defects, Molecular beam epitaxy, Equipment used, Film characteristics, SOI structure.

Unit 2: Oxidation: Growth mechanism & kinetics, Silicon oxidation model, Interface considerations, Orientation dependence of oxidation rates, thin oxides, Oxides, Oxidation technique & systems dry & wet oxidation., Masking properties of SiO2.

Unit 3: Diffusion: Diffusion from a chemical source in vapor form at high temperature, Diffusion from doped oxide source, Diffusion from an ion implanted layer.

Unit 4: Lithography: Optical lithography, Optical resists, Contact & proximity printing, Projection printing, Electron lithography, resists, Mask generation, Electron optics, Roster scans & vector scans, Variable beam shape, X-ray lithography, Resists & printing, X-ray sources &masks, Ion lithography.

Unit 5: Etching: Reactive plasma etching, AC & DC plasma excitation, Plasma properties, Chemistry & surface interactions, Feature size control & apostrophic etching, Ion enhanced & induced etching, Properties of etch processing. Reactive ion beam etching, Specific etches processes, poly/polycide, Trench etching.

Unit 6: Simulation & Analytical Techniques: Introduction to process modelling, SUPREM. Reliability issues in VLSI technology, Geometrical manipulations, A novel measurement technique for 2D implanted ion distributions, Introduction to partial differential equation solver, The merged multi grid method, Modeling & simulation of isothermal, Non isothermal and hydrodynamic devices.

Unit 7: MEMS Introduction and Historical Background, Scaling Effects. Micro/Nano Sensors, Actuators and Systems overview: Case studies. Review of Basic MEMS fabrication modules: Oxidation, Deposition Techniques, Lithography (LIGA), and Etching. Micromachining: Surface Micromachining, sacrificial layer processes, Stiction; Bulk Micromachining, Isotropic Etching and Anisotropic Etching, Wafer Bonding. Mechanics of solids in MEMS/NEMS: Stresses, Strain, Hookes's law, Poisson effect, Linear Thermal Expansion, Bending; Energy methods, Overview of Finite Element Method, Modeling of Coupled Electromechanical Systems.

Unit 8: MEMS types and their applications: Mechanical MEMS – Strain and pressure sensors, Accelerometers etc., Electromagnetic MEMS – Micromotors, Wireless and GPS MEMS etc Magnetic MEMS – all effect sensors, SQUID magnetometers, Optical MEMS – Micromachined fiber optic component, Optical sensors, Thermal MEMS – thermo-mechanical and thermo-electrical actuators, Peltier heat pumps.

Text/Reference Book:

- G. K. Ananthasuresh, K. J. Vinoy, S. Gopalkrishnan K. N. Bhat, V. K. Aatre, Micro and Smart Systems, Wiley India, 2012.
- S. E.Lyshevski, Nano-and Micro-Electromechanical systems: Fundamentals of Nano-and Microengineering (Vol. 8). CRC press, (2005).
- S. D. Senturia, Microsystem Design, Kluwer Academic Publishers, 2001.
- M. Madou, Fundamentals of Microfabrication, CRC Press, 1997.
- G. Kovacs, Micromachined Transducers Sourcebook, McGraw-Hill, Boston, 1998.

- M.H. Bao, Micromechanical Transducers: Pressure sensors, accelerometers, and Gyroscopes, Elsevier, New York, 2000

Course Outcomes: At the end of the course the students will be able to

1. Appreciate the underlying working principles of MEMS and NEMS devices.
2. Design and model MEM devices.
3. Explain the concept of molecular reorganization, fundamentals of surfaces and interfaces
4. Explain the different types of MEMS and its applications

VDP-117-V1 **Parallel Processing**

L T P	CR		
3 0 0	3	Theory	60
		Class Work	40
		Total	100
		Duration of Exam	3 Hrs.

Course Objectives:

- To learn the concept of parallel processing and implementation of pipelining.
- To introduce upcoming VLIW processors with case study of protocol applications.
- To introduce multithreaded architecture and discuss various issues & performance protocols.
- To familiarize with operating systems for multiprocessor systems

Syllabus Contents:

Unit 1: Overview of Parallel Processing and Pipelining, Performance analysis, Scalability

Unit 2: Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Software pipelining

Unit 3: VLIW processors Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC, MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture

Unit 4: Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions

Unit 5: Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues

Unit 6: Operating systems for multiprocessor systems, Customizing applications on parallel processing platforms

References:

- Kai Hwang, Faye A. Briggs, "Computer Architecture and Parallel Processing", MGH International Edition
- Kai Hwang, "Advanced Computer Architecture", TMH
- V. Rajaraman, L. Sivaram Murthy, "Parallel Computers", PHI.
- William Stallings, "Computer Organization and Architecture, Designing for performance" Prentice Hall, Sixth edition
- Kai Hwang, Zhiwei Xu, "Scalable Parallel Computing", MGH
- David Harris and Sarah Harris, "Digital Design and Computer Architecture", Morgan Kaufmann.

Course outcome:

At the end of this course, students will be able to

- Identify limitations of different architectures of computer
- Analysis quantitatively the performance parameters for different architectures
- Investigate issues related to compilers and instruction set based on type of architectures.
- Understand processing issues of operating systems for multiprocessor system.

VDP-119-V1 **System Design with Embedded Linux**

L T P	CR		
3 0 0	3	Theory	60
		Class Work	40
		Total	100
		Duration of Exam	3 Hrs.

Course Objectives:

- To introduce the students to Embedded Linux and Embedded Linux architecture.
- To introduce the students to embedded storage & devices.
- To introduce the students to real-time Linux.
- To introduce the students to embedded graphics

Syllabus Contents:

Unit 1: Embedded Linux Vs Desktop Linux, Embedded Linux Distributions

Unit 2: Embedded Linux Architecture, Kernel Architecture – HAL, Memory manager, Scheduler, File System, I/O and Networking subsystem, IPC, User space, Start-up sequence

Unit 3: Board Support Package, Embedded Storage: MTD, Architecture, Drivers, Embedded File System, Embedded Drivers: Serial, Ethernet, I2C, USB, Timer, Kernel Modules

Unit 4: Porting Applications: Real-Time Linux: Linux and real-time, Programming, Hard Real-time Linux

Unit 5: Building and Debugging: Kernel, Root file system, Embedded Graphics

Unit 6: Case study of uC Linux

References:

- Karim Yaghmour, "Building Embedded Linux Systems", O'Reilly & Associates
- P Raghvan, Amol Lad, Sriram Neelakandan, "Embedded Linux System Design and Development", Auerbach Publications
- Christopher Hallinan, "Embedded Linux Primer: A Practical Real World Approach", Prentice Hall, 2nd Edition, 2010.
- Derek Molloy, "Exploring BeagleBone: Tools and Techniques for Building with Embedded Linux", Wiley, 1st Edition, 2014.

Course outcome:

At the end of this course, students will be able to

- Familiarity with the embedded Linux development model.
- Write, debug, and profile applications and drivers in embedded Linux.
- Understand and create Linux BSP for a hardware platform

VDP-121-V1 **CAD of Digital System**

L T P	CR
3 0 0	3

Theory	60
Class Work	40
Total	100
Duration of Exam	3 Hrs.

Course Objectives:

- To introduce different VLSI design methodologies.
- To introduce VLSI automation tools.
- To learn the basics of general-purpose methods for optimization.
- To learn the concept of simulation & synthesis and implementation of simple circuits using RTL.

Syllabus Contents:

Unit 1: Introduction to VLSI Methodologies – Design and Fabrication of VLSI Devices, Fabrication Process and its impact on Design.

Unit 2: VLSI design automation tools – Data structures and basic algorithms, graph theory and computational complexity, tractable and intractable problems.

Unit 3: General purpose methods for combinational optimization – partitioning, floor planning and pin assignment, placement, routing.

Unit 4: Simulation – logic synthesis, verification, high level Synthesis.

Unit 5: MCMS-VHDL-Verilog-implementation of simple circuits using VHDL.

References:

- N.A. Sherwani, “Algorithms for VLSI Physical Design Automation”.
- S.H. Gerez, “Algorithms for VLSI Design Automation.

Course outcome:

At the end of this course, students will be able to

- Understand the different VLSI design methodologies.
- Understand different VLSI automation tools.
- Understand the basics of general method of alternation.
- Understand the concept of simulation and synthesis and implementation of simple circuit using RTL.

VDP-123-V1 **Device Modeling for Circuit Simulation**

L T P	CR		
3 0 0	3	Theory	60
		Class Work	40
		Total	100
		Duration of Exam	3 Hrs.

Course Objectives:

- To introduce about the basics of spice.
- To introduce about the modeling fundamental of semiconductor devices and circuits.
- To introduce about the various MOS models 1,2, Higher BSIM version.
- To Introduce about the advanced MOS Fabrication technologies.

Syllabus Contents:

Unit 1. Introduction to SPICE & MOS Fundamentals: Principle of circuit simulation and its objectives, AC, DC, Transient, Noise, Temperature etc analysis. MOS Threshold, transconductance with or without body bias Modeling & simulation, CMOS Inverters DC & AC Analysis, Pseudo-NMOS Inverters, Sizing inverters

Unit 2. Fabrication Simulation & Static Characterization: Introduction, IC Fabrication Technology: Overview of IC Fabrication Process, IC Photolithographic Process, Modeling the MOS Transistor for Circuit Simulations: MOS Models in SPICE, SPICE MOS LEVEL I Device Model with extraction of Parameters, Power Dissipation in CMOS Gates: Dynamic Power, Static Power, and Complete Power equation.

Unit 3. MOSFETS Modeling in Deep Sub-Micron: Introduction, Voltage Transfer Characteristics, Noise Margin Definitions for Single and Multiple source, NMOS transistors as Load Device: Saturated Enhancement Load, Linear Enhancement Load, BSIM3 Model: Binning Process in BSIM3, Short Channel Threshold Voltage, Mobility Model, Linear and saturation regions, sub-threshold current, Capacitance Model, Modeling Using Pass Transistor, CMOS Transmission Gate Logic.

Unit 4. Modeling of High Speed CMOS Design: Introduction, Switching time Analysis: Gate Sizing-Velocity saturation effects, Fanout Gate capacitance, Self- Capacitance calculations, Wire capacitance, Improving Delay Calculation with input slope, Gate sizing for Optimal Path Delay: Optimal Delay Problem, Inverter Chain Delay Optimization-FO4 Delay, Optimizing Paths with NANDs and NORs, Optimizing Paths with Logical Efforts: Derivation of Logical Effort, Understanding Logical Efforts, Branching Effort and Sideloads

Unit 5. Advanced MOS Technologies: Design and Manufacturing of Printed Electronics on Flexible substrate.

References:

1. Sedra and Smith, SPICE.
2. H.M. Rashid, Introduction to PSPICE, PHI.
3. B.G. Streetman & S. Baneerjee, Solid State Electronic Devices, PHI.
4. R. Raghuram, Computer Simulation of Electronic Circuits, Wiley Eastern Ltd.
5. Bar Lev, Basic Electronics

Course outcome:

At the end of this course, students will be able to

- Understand the basics of spice modeling.
- Understand the modeling & simulation of different MOS devices & circuits.
- Understand the analytical & simulation of different MOS performance parameter at DSM nodes.
- Understand the design challenges & fabrication issues in semiconductor technology.

VDP-105-V1 **RTL Simulation and Synthesis with PLDs Lab**

L T P	CR		
0 0 4	2	INT.	25
		EXT.	25
		Total	50
		Duration of Exam	3 Hrs.

List of Experiments:

1. Verilog implementation of basic digital gates.
2. Verilog implementation of 8:1 Mux/Demux.
3. Verilog implementation of Full Adder.
4. Verilog implementation of 8-bit Magnitude comparator.
5. Verilog implementation of Encoder/decoder.
6. Verilog implementation of Priority encoder.
7. Verilog implementation of Flip Flops.
8. Verilog implementation of 4-bit Shift registers (SISO, SIPO, PISO, bidirectional).
9. Verilog implementation of 3-bit Synchronous Counters.
10. Verilog implementation of Binary to Gray converter.
11. Verilog implementation of Parity generator.
12. Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines.
13. Vending machines - Traffic Light controller, ATM, elevator control.
14. PCI Bus & arbiter and downloading on FPGA.
15. UART/ USART implementation in Verilog.
16. Realization of single port SRAM in Verilog.
17. Verilog implementation of Arithmetic circuits like serial adder/ subtractor, parallel adder/subtractor, serial/parallel multiplier.
18. Discrete Fourier transform/Fast Fourier Transform algorithm in Verilog.

Course outcome:

At the end of the laboratory work, students will be able to:

- Identify, formulate, solve and implement problems in signal processing, communication systems etc using RTL design tools.
- Use EDA tools like Cadence, Mentor Graphics and Xilinx.

VDP-107-V1 **Microcontrollers and Programmable Digital Signal Processors Lab**

L T P	CR		
0 0 4	2	INT.	25
		EXT.	25
		Total	50
		Duration of Exam	3 Hrs.

List of Assignments:

Part A) Experiments to be carried out on Cortex-M3 development boards and using GNU tool chain

1. Blink an LED with software delay, delay generated using the SysTick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

Part B) Experiments to be carried out on DSP C6713 evaluation kits and using Code Composer Studio (CCS)

1. To develop an assembly code and C code to compute Euclidian distance between any two points
2. To develop assembly code and study the impact of parallel, serial and mixed execution
3. To develop assembly and C code for implementation of convolution operation
4. To design and implement filters in C to enhance the features of given input sequence/signal

Course Outcomes:

At the end of the laboratory work, students will be able to:

- Install, configure and utilize tool sets for developing applications based on ARM processor core SoC and DSP processor.
- Develop prototype codes using commonly available on and off chip peripherals on the Cortex M3 and DSP development boards.

VAC-301-V1 **Research Methodology and IPR**

L T P	CR		
3 0 0	3	Theory	60
		Class Work	40
		Total	100
		Duration of Exam	3 Hrs.

Course Objectives:

- To formulate a research problem and identify errors in the research problem.
- To learn approaches for effective literature survey.
- To prepare a presentation and research proposal.
- To learn about IPR, software and case studies regarding patents

Syllabus Contents:

Unit 1: Meaning of research problem, Sources of research problem, Criteria and characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, necessary instrumentation

Unit 2: Effective literature studies approaches, analysis, plagiarism, Research ethics.

Unit 3: Effective technical writing, how to write a report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

Unit 4: Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

Unit 5: Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

Unit 6: New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software, etc. Traditional knowledge Case Studies, IPR and IITs.

References:

- Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students"
- Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
- Ranjit Kumar, 2nd Edition, "Research Methodology: A Step-by-Step Guide for beginners"
- Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd, 2007.
- Mayall, "Industrial Design", McGraw Hill, 1992.
- Niebel, "Product Design", McGraw Hill, 1974.
- Asimov, "Introduction to Design", Prentice Hall, 1962.
- Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016.
- T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

Course outcome:

At the end of this course, students will be able to

- Understand that today's world is controlled by Computer, Information Technology, but tomorrow's world will be ruled by ideas, concepts, and creativity.
- Understand that when IPR takes such an important place in the growth of individuals & nation, it is needless to emphasize the need for information about Intellectual Property Rights to be promoted among students in general & engineering in particular.
- Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about economic growth and social benefits.

VDP-102-V1 **Analog and Digital CMOS VLSI Design**

L T P	CR		
3 0 0	3	Theory	60
		Class Work	40
		Total	100
		Duration of Exam	3 Hrs.

Course Objectives:

- To introduce the basic concepts of digital CMOS design & optimization of various design parameters.
- To familiarize the physical design algorithms for VLSI design.
- To introduce short channel effects, FINFET and metal gate technology.
- To familiarize differential amplifiers with various MOS loads & use of operational amplifiers in analog design.

Syllabus Contents:

Technology Scaling and Roadmap, Scaling issues, Standard 4 mask NMOS Fabrication process

Digital CMOS Design:

Unit 1: Review: Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models. Inverter: Static CMOS inverter, switching threshold and noise margin concepts and their evaluation, Dynamic behavior, Power consumption.

Unit 2: Physical design flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model. Combinational logic: Static CMOS design, Dynamic logic, Speed and power dissipation in dynamic logic, cascading dynamic gates,

Unit 3: Sequential logic: Static latches and registers, Bi-stability principle, MUX-based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, non-bistable sequential circuit. Advanced technologies: Giga-scale dilemma, short channel effects, High–k, Metal Gate technology, FinFET, TFET, etc.

Analog CMOS Design:

Unit 4: Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common gate stage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

Unit 5: Passive and active current mirrors: Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise

Unit 6: Operational amplifiers: One-stage OPAMP, two-stage OPAMP, Gain boosting, Common mode feedback, Slew rate, PSRR, Compensation of 2-stage OPAMP, Other compensation techniques.

Course Outcomes:

At the end of the course, students will be able to:

- Analyze, design, optimize and simulate analog and digital circuits using CMOS constrained by the design metrics.
- Connect the individual gates to form the building blocks of a system.
- Use EDA tools like Cadence, Mentor Graphics and other open source software tools like Ngspice.

References:

- J P Rabaey, A P Chandrakasan, B Nikolic, “Digital Integrated circuits: A design perspective”, Prentice Hall electronics and VLSI series, 2nd Edition.
- Baker, Li, Boyce, “CMOS Circuit Design, Layout, and Simulation”, Wiley, 2nd Edition.

- Behzad Razavi , “Design of Analog CMOS Integrated Circuits”, TMH, 2007.
- Phillip E. Allen and Douglas R. Holberg, “CMOS Analog Circuit Design”, Oxford, 3rd Edition.
- R J Baker, “CMOS circuit Design, Layout and Simulation”, IEEE Inc., 2008.
- Kang, S. and Leblebici, Y., “CMOS Digital Integrated Circuits, Analysis and Design”, TMH, 3rdEdition.
- Pucknell, D.A. and Eshraghian, K., “Basic VLSI Design”, PHI, 3rd Edition..

VDP-104-V1 **VLSI Design Verification and Testing**

L T P	CR		
3 0 0	3	Theory	60
		Class Work	40
		Total	100
		Duration of Exam	3 Hrs.

Course Objectives:

- To introduce the concept of testbench functionality & various types of testbench.
- To familiarize the various data types & use of data types in hardware description languages to develop digital systems.
- To introduce the subprograms: functions & procedures, use of subprograms in VLSI Testing.
- To familiarize the system verilog, basic OOP, object creation & utilization and randomization in SystemVerilog.

Syllabus Contents:

Unit 1: Verification guidelines: Verification Process, Basic Testbench functionality, directed testing, Methodology basics, Constrained-Random stimulus, Functional coverage, Testbench components, layered testbench, Building layered testbench, Simulation environment phases, Maximum code reuse, Testbench performance.

Unit 2: Data types: Built-in data types, Fixed-size arrays, Dynamic arrays, Queues, Associative arrays, Linked lists, Array methods, choosing a storage type, creating new types with typedef, Creating user-defined structures, Type conversion, Enumerated types, Constant strings, Expression width.

Unit 3: Procedural statements and routines: Procedural statements, tasks, functions and void functions, Routine arguments, Returning from a routine, Local data storage, Time values Connecting the testbench and design: Separating the testbench and design, Interface constructs, Stimulus timing, Interface driving and sampling, Connecting it all together, Top-level scope Program – Module interactions.

Unit 4: System Verilog Assertions: Basic OOP: Introduction, think of nouns, Not verbs, your first class, where to define a class, OOP terminology, Creating new objects, Object de-allocation, Using objects, Static variables vs. Global variables, Class methods, Defining methods outside of the class, Scoping rules, Using one class inside another, Understanding dynamic objects, Copying objects, Public vs. Local, Straying off course building a testbench.

Unit 5: Randomization: Introduction, What to randomize, Randomization in SystemVerilog, Constraint details, solution probabilities, Controlling multiple constraint blocks, Valid constraints, In-line constraints, The pre_randomize and post_randomize functions,

Unit 6: Random number functions, Constraints tips and techniques, Common randomization problems, Iterative and array constraints, Atomic stimulus generation vs. Scenario generation, Random control, Random number generators, Random device configuration.

References:

- Chris Spears, " System Verilog for Verification", Springer, 2nd Edition
- M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers
- IEEE 1800-2009 standard (IEEE Standard for SystemVerilog— Unified Hardware Design,Specification, and Verification Language).
- System Verilog website – www.systemverilog.org http://www.sunburstdesign.com/papers/CummingsSNUG2006Boston_SystemVerilog Events.pdf
- General reuse information and resources www.design-reuse.com
- OVM, UVM(on top of SV) www.verificationacademy.com
- Verification IP resources http://www.cadence.com/products/fv/verification_ip/pages/default.aspx

- http://www.synopsys.com/Tools/Verification/FunctionalVerification/VerificationIP/Pages/default.aspx

Course outcome:

At the end of this course, students will be able to

- Familiarity of Front end design and verification techniques and create reusable test environments.
- Verify increasingly complex designs more efficiently and effectively.
- Use EDA tools like Cadence, Mentor Graphics

VDP-112-V1 **Memory Technologies**

L T P	CR		
3 0 0	3	Theory	60
		Class Work	40
		Total	100
		Duration of Exam	3 Hrs.

Course Objectives:

- To introduce various types of memory Architectures.
- To introduce various performance parameters of memory Architectures.
- To introduce various memory packing technologies.
- To introduce about various 2D & 3D memory Architectures

Syllabus Contents:

Unit 1: Random Access Memory Technologies: Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

Unit 2: DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs, SRAM and DRAM Memory controllers.

Unit 3: Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

Unit 4: Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.

Unit 5: Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto-Resistive Random Access Memories (MRAMs), Experimental Memory Devices.

Unit 6: Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging

References:

- Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designs and Applications", Wiley Interscience
- Kiyoo Itoh, "VLSI memory chip design", Springer International Edition
- Ashok K Sharma, Semiconductor Memories: Technology, Testing and Reliability, PHI

Course Outcomes:

At the end of the course, students will be able to:

- Select architecture and design semiconductor memory circuits and subsystems.
- Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.
- Knowhow of the state-of-the-art memory chip design.
- Modeling & simulation of memory structure at different technology modes.

VDP-114-V1 **SoC Design**

L T P	CR		
3 0 0	3	Theory	60
		Class Work	40
		Total	100
		Duration of Exam	3 Hrs.

Course Objectives:

- To familiarize the basis of SOC design and its architectural issues.
- To familiarize the design flow and verification of ASIP's and NISC's along with various design methodologies.
- To introduce the functional simulation, synthesis, layout and timing analysis of single and multi core systems.
- To adapt the concept of voltage scaling & optimization of various design parameters oon the basis of case studies.

Syllabus Contents:

Unit 1: ASIC

- Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and their impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

Unit 2: NISC

- NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction set Processors (ASIP), No-Instruction-Set-computer (NISC) design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

Unit 3: Simulation

- Different simulation models, behavioural, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, low-power FPGA, Reconfigurable systems, SoC-related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

Unit 4: Low power SoC design / Digital system,

- Design synergy, low-power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

Unit 5: Synthesis

- Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails, paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology-independent and technology-dependent approaches for synthesis, optimization constraints, Synthesis report analysis. Single core and multi-core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, fault-tolerant designs

Unit 6: Case study for overview of cellular phone design with emphasis on area optimization, speed improvement and power minimization.

Note: Students will prepare and present a term paper on relevant identified current topics (in batches of three students per topic) as a part of the theory course.

References:

- Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.
- B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006
- Rochit Rajsuman, "System-on- a-chip: Design and test", Advantest America R & D Center, 2000

- P Mishra and N Dutt, “Processor Description Languages”, Morgan Kaufmann, 2008
- Michael J. Flynn and Wayne Luk, “Computer System Design: System-on-Chip”. Wiley, 2011

Course Outcomes:

At the end of the course, students will be able to:

- Identify and formulate a given problem in the framework of SoC based design approaches
- Design SoC based system for engineering applications
- Realize impact of SoC on electronic design philosophy and Macro-electronics thereby incline towards entrepreneurship & skill development.

VDP-116-V1 **Low Power VLSI Design**

L T P	CR		
3 0 0	3	Theory	60
		Class Work	40
		Total	100
		Duration of Exam	3 Hrs.

Course Objectives:

- To introduce the need for low-power designing
- To learn about SPICE simulation
- To learn about leakage control at circuit & architecture level
- To learn about the clock distribution networks

Syllabus Contents:

Unit 1: Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree Of freedom, recurring themes in low-power, emerging low-power approaches, dynamic dissipation in CMOS, effects of Vdd & Vt on speed, constraints on Vt reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations.

Unit 2: Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high-performance approaches.

Unit 3: Low Power Clock Distribution: Power dissipation in clock distribution, single driver Versus distributed buffers, buffers & device sizing under process variations, zero skew Vs. tolerable skew, chip & package co-design of clock network.

Unit 4: Logic Synthesis for Low Power estimation techniques: Power minimization techniques, low-power arithmetic components- circuit design styles, adders, multipliers.

Unit 5: Low Power Memory Design: Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits.

Unit 6: Low Power Microprocessor Design System: power management support, architectural trade-offs for power, choosing the supply voltage, low-power clocking, implementation problems for low power, comparison of microprocessors for power & performance.

References:

- P. Rashinkar, Paterson and L. Singh, “Low Power Design Methodologies”, Kluwer Academic, 2002
- Kaushik Roy, Sharat Prasad, “Low power CMOS VLSI circuit design”, John Wiley sons Inc.,2000.
- J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley, 1999.
- A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer,1995
- Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.

Course Outcomes:

At the end of the course, students will be able to:

- CO1: Identify the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability.
- CO2: Characterize and model power consumption & understand the basic analysis methods.
- CO3: Understand leakage sources and reduction techniques.

VDP-118-V1 **CMOS RF Circuit Design**

L T P	CR		
3 0 0	3	Theory	60
		Class Work	40
		Total	100
		Duration of Exam	3 Hrs.

Course Objectives:

- To introduce the concept of RF design and wireless technology.
- To learn the basics of RF modulation and RF testing.
- To introduce the behaviors of BJT & MOSFET at RF Frequencies.
- To familiarize the RF circuit design concept.

1. Introduction to RF design and Wireless Technology

Design and applications, Complexity and choice of Technology, Basic concepts in RF design, Nonlinearity and time Variance, Inter-symbol interference, Random processes and noise. Sensitivity and dynamic range, Conversion of gains and distortion.

2. RF Modulation

Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, Mobile RF communication and basics of Multiple Access techniques. Receiver and Transmitter architectures, Direct conversion and two-step transmitters.

3. RF Testing

RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub-sampled receivers.

4. BJT and MOSFET Behavior at RF Frequencies

BJT and MOSFET behavior at RF frequencies, Modeling of the transistors and SPICE model, Noise performance and limitations of devices, Integrated parasitic elements at high frequencies and their monolithic implementation

5. RF Circuits Design

Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation, Low-noise amplifier design in various technologies, Design of Mixers at GHz frequency range, Various mixers working and implementation. Oscillators- Basic topologies, VCO and definition of phase noise, Noise power and trade-off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design, Liberalization techniques, Design issues in integrated RF filters.

References:

- Thomas H. Lee, Design of CMOS RF Integrated Circuits, Cambridge University press 1998.
- B. Razavi, RF Microelectronics, PHI 1998
- R. Jacob Baker, H.W. Li, D.E. Boyce, CMOS Circuit Design, layout and Simulation, PHI, 1998.
- Y.P. Tsividis, Mixed Analog and Digital Devices and Technology, TMH, 1996

Course Outcomes:

At the end of the course, students will be able to:

- Understand the concept of RF circuit design.
- Understand the basis of RF modulation and RF testing.
- Understand the behaviors of BJT & MOSFET at RF frequency.
- Design simple RF circuits.

VDP-120-V1 **Communication Buses and Interfaces**

L T P	CR
3 0 0	3

Theory	60
Class Work	40
Total	100
Duration of Exam	3 Hrs.

Course Objectives:

- To introduce various serial, inter-fall, and design applications.
- To introduce CAN and PCI protocols.
- To introduce the development of an API for data transfer on serial bus.
- To teach students the design and development of peripherals to do data transfer.

Syllabus Contents:

Unit 1: Serial Buses: Physical interface, Data and Control signals, features,
Unit 2: limitations and applications of RS232, RS485, I2C, SPI
Unit 3: CAN - Architecture, Data transmission, Layers, Frame formats, applications
Unit 4: PCIe - Revisions, Configuration space, Hardware protocols, applications
Unit 5: USB - Transfer types, enumeration, Descriptor types and contents, Device driver
Unit 6: Data Streaming Serial Communication Protocol, Serial Front Panel Data Port (SFPDP) using fibre optic and copper cable

References

- Jan Axelson, "Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems", Lakeview Research, 2nd Edition
- Jan Axelson, "USB Complete", Penram Publications
- Mike Jackson, Ravi Budruk, "PCI Express Technology", Mindshare Press
- Wilfried Voss, "A Comprehensible Guide to Controller Area Network", Copperhill Media Corporation, 2nd Edition, 2005.
- Serial Front Panel Draft Standard VITA 17.1 – 200x
- Technical references on www.can-cia.org, www.pcisig.com, www.usb.org

Course Outcomes:

At the end of the course, students will be able to:

- Select a particular serial bus suitable for a particular application.
- Develop APIs for configuration, reading and writing data onto serial bus.
- Design and develop peripherals that can be interfaced to desired serial bus.

VDP-122-V1 **Network Security and Cryptography**

L T P	CR		
3 0 0	3	Theory	60
		Class Work	40
		Total	100
		Duration of Exam	3 Hrs.

Course Objectives:

- To introduce basic and advanced concepts of security.
- To introduce various cryptography techniques.
- To teach students various authentication techniques.
- To introduce various threats.

Syllabus Contents:

Unit 1: Security Need, security services, Attacks, OSI Security Architecture, one-time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques.

Unit 2: Number Theory - Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

Unit 3: Private-Key (Symmetric) Cryptography - Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

Unit 4: Public-Key (Asymmetric) Cryptography - RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4, MD5, Secure Hash Algorithm, RIPEMD-160, HMAC.

Unit 5: Authentication - IP and Web Security: Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP Security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer and Transport Layer Security, Secure Electronic Transaction.

Unit 6: System Security - Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Countermeasures, Firewalls, Firewall Design Principles, Trusted Systems.

References:

- William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition.
- Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communication in a Public World", Prentice Hall, 2nd Edition
- Christopher M. King, Ertem Osmanoglu, Curtis Dalton, "Security Architecture, Design Deployment and Operations", RSA Press.
- Stephen Northcutt, Leny Zeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, Inside Network Perimeter Security", Pearson Education, 2nd Edition
- Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident Detection and Response", William Pollock Publisher, 2013.

Course Outcomes:

At the end of the course, students will be able to:

- Identify and utilize different forms of cryptography techniques.
- Incorporate authentication and security in network applications.
- Distinguish among different types of threats to the system and handle the same.

VDP-124-V1 **VLSI Signal Processing**

L T P	CR
3 0 0	3

Theory	60
Class Work	40
Total	100
Duration of Exam	3 Hrs.

Course Objectives:

- To give knowledge about DSP algorithms.
- To explain retiming techniques, folding and register minimization path problem.
- To introduce algorithm strength reduction techniques & parallel processing of FIR and IIR filters.
- To explain finite word length effects and round-off noise computation in DSP.

Syllabus Contents:

Unit 1: Introduction to DSP systems, Pipelined and parallel processing.

Unit 2: Iteration Bound, Retiming, unfolding, algorithmic strength reduction in filters and Transforms.

Unit 3: Systolic architecture design, fast convolution, pipelined and parallel recursive and adaptive filters, scaling and round-off noise.

Unit 4: Digital lattice filter structures, bit-level arithmetic, architecture, redundant arithmetic.

Unit 5: Numerical strength reduction, synchronous, wave and asynchronous pipelines, low power design.

Unit 6: Programmable digital signal processors.

References:

- Keshab K. Parthi[A1] , VLSI Digital signal processing systems, design and implementation[A2] , Wiley, Inter Science, 1999.
- Mohammad Isamail and Terri Fiez, Analog VLSI signal and information processing, McGraw Hill, 1994
- S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall, 1985.

Course outcome:

At the end of this course, students will be able to

- Acquired knowledge about DSP algorithms, its DFG representation, pipelining and parallel processing approaches.
- Ability to acquire knowledge about retiming techniques, folding and register minimization path problems.
- Ability to have knowledge about algorithmic strength reduction techniques and parallel
- Ability to have knowledge about algorithmic strength reduction techniques and parallel Processing of FIR and IIR digital filters.
- Acquired knowledge about finite word-length effects and round off noise computation in DSP systems.

VDP-126-V1 **ASIC's & FPGA**

L T P	CR
3 0 0	3

Theory	60
Class Work	40
Total	100
Duration of Exam	3 Hrs.

Course Objectives:

- To familiarize the use of hardware description language in ASIC's & FPGAs.
- To introduce the various types of ASICs its design, how & various programmable logic devices.
- To familiarize the FPGA & implementation of digital logic on programmable logic devices.
- To introduce the physical design algorithms and the role of testing in VLSI design.

Syllabus Contents:

Unit 1: Introduction to hardware description languages: Introduction to VHDL, types of modeling, dataflow modeling, behavioral modeling, structural modeling, use of package for structural modeling, finite state machine modeling.

Unit 2: Introduction to ASICs: Introduction to ASICs, ASIC design flow, types of ASICs, full custom ASIC's, standard cell-based ASIC's, Gate array based ASIC's, channeled gate array, structured gate arrays, programmable logic devices, introduction to programmable logic, fixed versus programmable logic, programmable logic devices, types of programmable logic devices, PROMs, PLA, PAL, CPLD & FPGA.

Unit 3: Introduction to FPGA: Introduction to FPGA, evolution of programmable devices, conceptual diagram of a typical FPGA, Logic blocks, interconnection resources, FPGA versus ASIC, applications of FPGA, FPGA design flow, and implementation process.

Unit 4: FPGA Architecture: Various classes of FPGAs, symmetrical array, row-based, hierarchical PLD, sea-of-gates. Programming technologies, static RAM programming technology, anti-fuse programming technology, EPROM and EEPROM programming technology, commercially available FPGAs, general architecture of Xilinx FPGAS, CLB Interconnect.

Unit 5: Physical Design: Circuit partitioning algorithm, K-L algorithm, floor planning algorithm, cluster growth roof planning, introduction to placement & routing.

Unit 6: VLSI Testing: Basic concepts of testing, yield and reject rate, ATPG, ATPG design flow, various stuck-at faults, BIST.

Course Outcomes:

At the end of this course, students will be able to

- To understand the VHDL language & its programming.
- To understand the ASICs & FPGAS & the implementation of digital logic these devices.
- To understand the concept of FPGA, various types of FPGAS & its architecture.
- To understand physical design algorithms & various testing techniques.

VDP-106-V1 **Analog and Digital CMOS VLSI Design Lab**

L T P	CR		
0 0 4	2	INT.	25
		EXT.	25
		Total	50
		Duration of Exam	3 Hrs.

List of Experiments:

1. Use V_{DD}=1.8V for 0.18um CMOS process, VDD=1.3V for 0.13um CMOS Process, and V_{DD}=1V for 0.09um CMOS Process.
   a) Plot I_D vs. V_{GS} at different drain voltages for NMOS, PMOS.
   b) Plot I_D vs. V_{GS} at particular drain voltage (low) for NMOS, PMOS and determine Vt.
   c) Plot I_D vs. V_{GS} at particular gate voltage (high) for NMOS, PMOS and determine I_{OFF} and sub-threshold slope.
   d) Plot I_D vs. V_{DS} at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
   e) Extract V_{th} of NMOS/PMOS transistors (short channel and long channel). Use VDS =30mV

   To extract Vth use the following procedure.
   i. Plot gm vs V_{GS} using NGSPICE and obtain peak gm point.
   ii. Plot y=ID/(gm)1/2 as a function of VGS using Ngspice.
   iii. Use Ngspice to plot tangent line passing through peak gm point in y (VGS) plane and determine Vth.
   f) Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency.

   Tabulate your result according to technologies and comment on it.

2. Use VDD=1.8V for 0.18um CMOS process, VDD=1.2V for 0.13um CMOS Process and VDD=1V for 0.09um CMOS Process.
   a) Perform the following
      i. Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter.
      ii. Plot VTC for CMOS inverter with varying VDD.
      iii. Plot VTC for CMOS inverter with varying device ratio.
   b) Perform transient analysis of CMOS inverter with no load and with load and determine tpHL, tpLH, 20%-to-80% tr and 80%-to-20% tf. (use VPULSE = 2V, Cload = 50fF) Perform AC analysis of CMOS inverter with fanout 0 and fanout 1. (Use Cin= 0.012pF, Cload = 4pF, Rload = k)
3. Use Ngspice to build a three stage and five stage ring oscillator circuit in 0.18um and 0.13um technology and compare its frequencies and time period.
4. Perform the following
   a) Draw small signal voltage gain of the minimum-size inverter in 0.18um and 0.13um technology as a function of input DC voltage. Determine the small signal voltage gain at the switching point using Ngspice and compare the values for 0.18um and 0.13um process.
   b) Consider a simple CS amplifier with active load, as explained in the lecture, with NMOS transistor MN as driver and PMOS transistor MP as load, in 0.18um technology. (W/L)MN=5, (W/L)MP=10 and L=0.5um for both transistors.

i. Establish a test bench, as explained in the lecture, to achieve VDSQ=VDD/2.
ii. Calculate input bias voltage if bias current=50uA.
iii. Use Ngspice and obtain the bias current. Compare its value with 50uA.
iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier using small signal analysis in Ngspice (consider 30fF load capacitance).
v. Plot step response of the amplifier for input pulse amplitude of 0.1V. Derive time constant of the output and compare it with the time constant resulted from -3dB BW
vi. Use Ngspice to determine input voltage range of the amplifier

5. Three OPAMP INA. Vdd=1.8V Vss=0V, CAD tool: Mentor Graphics DA. Note: Adjust accuracy options of the simulator (setup->options in GUI). Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.
   i. Draw the schematic of op-amp macro model.
   ii. Draw the schematic of INA.
   iii. Obtain parameters of the op-amp macro model such that
      a. low-frequency voltage gain = 5x104,
      b. unity gain BW (fu) = 500KHz,
      c. input capacitance=0.2pF,
      d. output resistance =_,
      e. CMRR=120dB
   iv. Draw schematic diagram of CMRR simulation setup.
   v. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).
   vi. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.
   vii. Repeat (iii) to (vi) by considering CMRR of all OPAMPs to be 90dB.
6. Technology: UMC 0.18um, VDD=1.8V. Use MAGIC or Microwind.
   a) Draw layout of a minimum size inverter in UMC 0.18um technology using MAGIC Station layout editor. Use that inverter as a cell and lay out three cascaded minimum-sized inverters. Use M1 as interconnect line between inverters.
   b) Run DRC, LVS and RC extraction. Make sure there is no DRC error. Extract the netlist.
   c) Use extracted netlist and obtain tPHLtPLH for the middle inverter using Eldo.
   d) Use interconnect length obtained and connect the second and third inverter.
   Extract the new netlist and obtain tPHL and tPLH of the middle inverter. Compare new values of delay times with corresponding values obtained in part ‘c’.

Course Outcomes:

At the end of the laboratory work, students will be able to:

- Design digital and analog Circuit using CMOS.
- Use EDA tools like Cadence, Mentor Graphics and other open source software tools like Ngspice

VDP-108-V1 **VLSI Design Verification and Testing Lab**

L T P	CR		
0 0 4	2	INT.	25
		EXT.	25
		Total	50
		Duration of Exam	3 Hrs.

List of Assignments:

1. Sparse memory
2. Semaphore
3. Mail box
4. Classes
5. Polymorphism
6. Coverage
7. Assertions

Course Outcomes: At the end of the laboratory work, students will be able to:

- Verify increasingly complex designs more efficiently and effectively.
- Use EDA tools like Cadence, Mentor Graphics.

ENGLISH FOR RESEARCH PAPER WRITING (AEC-301-V1)

L T P CR			
2 0 0 0	**Theory**	:	**60**
	Class Work	:	**40**
	Total	:	**100**
	Duration of Exam	:	**3 Hrs.**

Course objectives:

- Understand how to improve your writing skills and level of readability
- Learn about what to write in each section
- Understand the skills needed when writing a title. Ensure the good quality of the paper at the very first submission

Unit 1: Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

Unit 2: Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction

Unit 3: Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

Unit 4: Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature,

Unit 5: Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions

Unit 6: Useful phrases, how to ensure the paper is as good as it could possibly be for the first-time submission

Suggested Studies:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's

Book.

1. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

DISASTER MANAGEMENT (VAC-302-V1)

L T P CR			
2 0 0 0	**Theory**	:	**60**
	Class Work	:	**40**
	Total	:	**100**
	Duration of Exam	:	**3 Hrs.**

Course Objectives:

- Learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in

Syllabus

Unit1: Introduction: Disaster: Definition, Factors And Significance; Difference Between Hazard And Disaster; Natural And Manmade Disasters: Difference, Nature, Types And Magnitude.

Unit 2: Repercussions Of Disasters And Hazards: Economic Damage, Loss Of Human And Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.

Unit 3: Disaster Prone Areas In India: Study Of Seismic Zones, Areas Prone To Floods And Droughts, Landslides And Avalanches, Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami, Post-Disaster Diseases And Epidemics.

Unit 4: Disaster Preparedness And Management: Preparedness, Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk, Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports, Governmental And Community Preparedness.

Unit 5: Risk Assessment: Disaster Risk: Concept And Elements, Disaster Risk Reduction, Global And National Disaster Risk Situation, Techniques of Risk Assessment, Global Co-Operation In Risk Assessment And Warning, People's Participation In Risk Assessment. Strategies for Survival.

Unit 6: Disaster Mitigation: Meaning, Concept And Strategies Of Disaster Mitigation, Emerging Trends in Mitigation, Structural Mitigation And Non-Structural Mitigation, Programs of Disaster Mitigation In India.

SUGGESTED READINGS:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "' New Royal Book Company.
2. Sahni, Pardeep et al. (Eds.), "Disaster Mitigation Experiences And Reflections", Prentice Hall Of India, New Delhi.
3. Goel S. L., Disaster Administration And Management: Text And Case Studies", Deep &Deep Publication Pvt. Ltd., New Delhi.

SANSKRIT FOR TECHNICAL KNOWLEDGE (AEC-302-V1)

L T P CR			
2 0 0 0	**Theory**	:	**60**
	Class Work	:	**40**
	Total	:	**100**
	Duration of Exam	:	**3 Hrs.**

Course Objectives

- To get a working knowledge of illustrious Sanskrit, the scientific language in the world
- Learning Sanskrit to improve brain functioning
- Learning Sanskrit to develop logic in mathematics, science & other subjects, enhancing memory power
- The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature

Syllabus

Unit 1: Alphabets in Sanskrit, Past/Present/Future Tense, Simple Sentences

Unit 2: Order, Introduction of roots, technical information about Sanskrit Literature

Unit 3: Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

Suggested reading

1. "Abhyaspustakam" – Dr.Vishwas, Samskrita-Bharti Publication, New Delhi
2. "Teach Yourself Sanskrit" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication
3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi.

Course Output

1. Understanding basic Sanskrit language
2. Ancient Sanskrit literature about science & technology can be understood
3. Being a logical language will help to develop logic in students

VALUE EDUCATION (VAC-303-V1)

L T P CR			
2 0 0 0	**Theory**	**:**	**60**
	Class Work	**:**	**40**
	Total	**:**	**100**
	Duration of Exam	**:**	**3 Hrs.**

Course Objectives

- Understand the value of education and self- development
- Imbibe good values in students
- Let them know about the importance of character

Unit 1: Values and self-development, social values and individual attitudes, Work ethics, Indian vision of humanism, Moral and non-moral valuation. Standards and principles, Value judgements

Unit 2: Importance of cultivation of values, Sense of duty. Devotion, Self-reliance. Confidence, Concentration, Truthfulness, Cleanliness, Honesty, Humanity. Power of faith, National Unity, Patriotism. Love for nature, Discipline

Unit 3: Personality and Behavior Development, Soul and Science, attitude, positive thinking, integrity and discipline, Punctuality, Love and Kindness, Avoid fault Thinking, Free from anger, Dignity of labour, Universal brotherhood and religious tolerance, True friendship,□Happiness Vs suffering, love for truth, Aware of self-destructive habits, Association and Cooperation, doing best for saving nature

Unit 4: Character and Competence, Holy books vs Blind faith, Self-management and Good health, Science of reincarnation, Equality, Nonviolence, Humility, Role of Women, All religions and same message, Mind your Mind, Self-control, Honesty, Studying effectively

Suggested reading

1. Chakroborty, S.K. “Values and Ethics for organizations: Theory and practice”, Oxford University Press, New Delhi

Course outcomes

- Knowledge of self-development
- Learn the importance of Human values
- Developing the overall personality

CONSTITUTION OF INDIA (VAC-112-V1)

L T P CR			
2 0 0 0	**Theory**	:	**60**
	Class Work	:	**40**
	Total	:	**100**
	Duration of Exam	:	**3 Hrs.**

Course Objectives:

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.

Syllabus

Unit 1: History of Making of the Indian Constitution: History**,** Drafting Committee (Composition & Working)

Unit 2: Philosophy of the Indian Constitution: Preamble, Salient Features.

Unit 3: Contours of Constitutional Rights & Duties: Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

Unit 4: Organs of Governance: Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions

Unit 5: Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation, Panchayati raj, Introduction, PRI: Zila Panchayat, Elected officials and their roles, CEO Zila Pachayat, Position and role, Block level, Organizational Hierarchy (Different departments), Village level, Role of Elected and Appointed officials, Importance of grass root democracy

Unit 6: Election Commission: Election Commission, Role and Functioning, Chief Election Commissioner and Election Commissioners, State Election Commission, Role and Functioning, Institutions and Bodies for the welfare of SC/ST/OBC and women.

Course Outcomes:

- Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
- Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
- Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
- Discuss the passage of the Hindu Code Bill of 1956.

Suggested reading

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

PEDAGOGY STUDIES (VAC-304-V1)

L T P CR			
2 0 0 0	**Theory**	**:**	**60**
	Class Work	**:**	**40**
	Total	**:**	**100**
	Duration of Exam	**:**	**3 Hrs.**

Course Objectives:

1. Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
2. Identify critical evidence gaps to guide the development.

Unit 1: Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology, Theories of learning, Curriculum, Teacher education, Conceptual framework, Research questions**,** Overview of methodology and searching,

Unit 2: Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries, Curriculum, Teacher education.

Unit 3: Evidence on the effectiveness of pedagogical practices, Methodology for the in-depth stage: quality assessment of included studies, How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? Theory of change, Strength and nature of the body of evidence for effective pedagogical practices, Pedagogic theory and pedagogical approaches, Teachers' attitudes and beliefs and Pedagogic strategies.

Unit 4: Professional development: alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the community, Curriculum and assessment, Barriers to learning: limited resources and large class sizes

Unit 5: Research gaps and future directions: Research design, Contexts, Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact.

Course Outcomes:

Students will be able to understand:

- What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
- What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
- How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

Suggested reading

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal, Educational Development, 33 (3): 272–282.

5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, ‘learning to read’ campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

STRESS MANAGEMENT BY YOGA (AEC-317-V1)

L T P CR			
2 0 0 0	**Theory**	:	**60**
	Class Work	:	**40**
	Total	:	**100**
	Duration of Exam	:	**3 Hrs.**

Course Objectives

- To achieve overall health of body and mind
- To overcome stress

Syllabus

Unit 1: Definitions of the eight parts of yog. (Ashtanga)

Unit 2: Yam and Niyam, do's and Don't's in life, i) Ahinsa, satya, astheya, bramhacharya and aparigraha, ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan

Unit 3: Asan and Pranayam, i) Various yog poses and their benefits for mind & body, ii) Regularization of breathing techniques and its effects-Types of pranayam

Course Outcomes:

- Develop a healthy mind in a healthy body, thus improving social health also
- Improve efficiency

Suggested reading

1. 'Yogic Asanas for Group Training-Part-I": Janardan Swami Yogabhyasi Mandal, Nagpur
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS (AEC-304-V1)

L T P CR			
2 0 0 0	**Theory**	**:**	**60**
	Class Work	**:**	**40**
	Total	**:**	**100**
	Duration of Exam	**:**	**3 Hrs.**

Course Objectives:

- To learn to achieve the highest goal happily
- To become a person with a stable mind, pleasing personality and determination
- To awaken wisdom in students

Unit 1: Neetisatakam-Holistic development of personality, Verses 19,20,21,22 (wisdom), Verses 29,31,32 (pride & heroism), Verses 26,28,63,65 (virtue), Verses 52,53,59 (dont's), Verses 71,73,75,78 (do's)

Unit 2: Approach to day-to-day work and duties, Shrimad Bhagwad Geeta, Chapter 2-Verses 41, 47,48, Chapter 3 Verses 13, 21, 27, 35, Chapter 6 Verses 5,13,17, 23, 35, Chapter 18 Verses 45, 46, 48.

Unit 3: Statements of basic knowledge, Shrimad Bhagwad Geeta: Chapter2 Verses 56, 62, 68**,** Chapter 12 Verses 13, 14, 15, 16,17, 18**,** Personality of Role model. Shrimad Bhagwad Geeta, Chapter2 Verses 17, Chapter3 Verses 36,37,42, Chapter4 Verses 18, 38,39**,** Chapter18 Verses 37,38,63

Course Outcomes:

- Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
- The person who has studied Geeta will lead the nation and mankind to peace and prosperity
- Study of Neetishatakam will help in developing a versatile personality of students.

Suggested reading

1. "Srimad Bhagavad Gita" by Swami Swarupananda, Advaita Ashram (Publication Department), Kolkata
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.

SWAMI VIVEKANANDA'S THOUGHTS (AEC-305-V1)

L T P CR			
2 0 0 0	**Theory**	:	**60**
	Class Work	:	**40**
	Total	:	**100**
	Duration of Exam	:	**3 Hrs.**

Course Objectives:

- To introduce the biography and philosophical thought of Swami Vivekananda
- To present Swami Vivekananda's views on major religions of the world and Universal Religion
- To present Swami Vivekananda's teachings and views on social issues.

Syllabus

Unit 1: Swami Vivekananda: a Brief biography, Influence of Ramakrishna on Vivekananda, Parliament of Religions, Establishment of Ramakrishna Mission.

Unit 2: Philosophy of Swami Vivekananda, Nature of Reality, Nature of Self, Nature of the universe, The doctrine of Maya, Identity of Self and God, Karma Yoga, Raj Yoga, Bhakti Yoga, Gyan Yoga.

Unit 3: Swami Vivekananda's observations on major religions of the world (a) Hinduism (b) Christianity (c) Islam

Unit 4: The concept of Universal Religion and its characteristics, Fundamental unity of all religions, acceptance and not tolerance is the principle.

Unit 5: Vivekananda and Nationalism, The message of patriotism, spirituality as the basis of patriotism, Sociological views of Vivekananda, His views on caste and untouchability, status of women, His views on Education, Swami Vivekananda's concept of Vedantic Socialism

Books: The Complete Works of Swami Vivekananda Vol. 1 to 8 Relevant Chapters

Annexure-A

J.C. Bose University of Science & Technology, YMCA, Faridabad
(A Haryana State Government University)
(Established by Haryana State Legislative Act No. 21 of 2009 & Recognized by UGC Act 1956 u/s 22 to Confer Degrees)
Accredited 'A' Grade by NAAC

Implementation of Credit Transfer/Mobility Policy of online courses

Reference: Gazette of India (Extraordinary) Part-III, Section-4 No. 295, UGC **(Credit Framework for Online Learning Courses through SWAYAM) Regulation, 2016,** dated 19/07/2016.

With reference to 12th Academic Council Meeting dated 03/05/2017 (Agenda Item No. AC/11/12), wherein MOOCs were adopted in the CBCS scheme, In continuation to that, following modalities are proposed to introduce the credit transfer policy in academic curriculum for the Massive Open Online Courses (MOOC's) offered through SWAYAM (Study Webs of Active-Learning for Young Aspiring Minds) Portal.

A. General Guidelines

1. The SWAYAM shall notify in June and November every year, the list of the online learning Courses going to be offered in the forthcoming Semester on its website https://swayam.gov.in.
2. All the UTDs/Affiliated Colleges shall, within 4 weeks from the date of notification by SWAYAM, consider through their Chairperson/Principal the online learning courses being offered through the SWAYAM platform; and keeping in view their academic requirements, decide upon the courses which it shall permit for credit transfer and keeping in view the following points:

    a) There is non-availability of suitable teaching staff for running a course in the Department.
    b) The facilities for offering the elective papers (courses), sought for by the students are not on offer/scheme in the Institution, but are available on the SWAYAM platform.
    c) The courses offered on SWAYAM would supplement the teaching-learning process in the Institution.
    d) Online courses through SWAYAM should not be more than 20% of total courses offered in a particular semester of a programme.
3. The courses offered in a particular semester will be compiled by Digital India Cell as decided and forwarded by concerned UTDs and affiliated colleges in the prescribed format to digitalindia.ymca@gmail.com and compiled set will be put up in Academic Council for approval.
4. Student can opt for 12-16 weeks course equivalent to 3-6 credits under mentorship of faculty (MHRD MOOC's guidelines 11.1(J) issued by the MHRD vide its orders dated 11/03/2016).

5. Every student being offered a particular paper (course) would be required to register for the MOOCs for that course/paper on SWAYAM through University's/Affiliated College's SWAYAM-NPTEL Local Chapter.
6. The UTD/College may designate a faculty member as course coordinator/mentor to guide the students (at least 20 students) throughout the course with 2 hours per week contribution and with mentor addition on the Local Chapter. The mentor Chairperson/Principal will ensure the provision of facilities for smooth running of the course viz. Internet facility and proper venue in the department/college.
7. Digital India Cell of the University will be the Nodal point for keeping track of MOOCs enrolments in the University and the concerned chairpersons/principals are expected to aware their students/faculty about the online courses.
8. Importance of online learning and credit transfer policy must be shared with the students at entry level by the concerned department/college. Same may be incorporated during induction program for newly admitted students.
9. The departmental/college MOOC coordinators appointed by chairpersons of concerned departments/Principals of affiliated colleges will be responsible for identification of relevant MOOCs in the UTDs/Colleges and smooth conduction during the course.

B. Credit Transfer/Mobility of MOOCs

1. The parent Institution (offering the Course) shall give the equivalent credit weightage to the students for the credits earned through online learning courses through SWAYAM platform in the credit plan of the program.
2. Following pattern will be followed for distribution of credits and will be applicable to all students from Jan 2018 onwards:

Program	**Duration**	**Minimum Credits to be earned***
B.Tech	Semester I to VIII	3
M.Tech/MBA/M.Sc./MA	Semester I to IV	3
BBA/BCA/B.Sc./BA	Semester I to VI	3

***All students of UTDs/Affiliated colleges of all courses have to mandatorily earn minimum prescribed credits.**

<u>Note:</u> From session 2019-20 onwards, for B.Tech program, a student has to earn at least 12 credits during the duration of the Degree subject to the passing of at least one MOOC course (carrying minimum 3 credits per year).

3. A student will be eligible to get Under-Graduate/Post-Graduate degree (B.Tech/M.Tech) with Honours if he/she completes additional credits through MOOC's. (AICTE Model Curriculum, Chapter1(B)). Following pattern will be followed for earning additional credits for the award of Honours degree:

Program	Duration	Credits to be earned*	Minimum CGPA
B.Tech	Semester I to VIII	12	8.0
M.Tech	Semester I to IV	6	8.0

*Inclusive of *Minimum credits to be earned* mentioned in clause B(2) above.

4. The earned credits shall be accepted and transferred to the total credits of the concerned students by the University for Completion of his/her degree. Credits earned through MOOCs will be incorporated in the mark sheet issued to the student by Controller of Examination.
5. Credits for MOOC's will be verified by the concerned department/college and will be forwarded to Controller of Examination for further processing.
6. The courses where model curriculum of AICTE is not applicable, pattern laid down as in B(2) will be followed.

NOTE:

1. These guidelines will be applicable to all Affiliating institutions under University along with all UTDs. Affiliating colleges will establish their own Local Chapter on SWAYAM and follow the same process.
2. For further clarifications, Notifications "Credit Framework for Online Learning Courses through SWAYAM" (UGC Regulations dated 19/07/2016) and "MHRD MOOC's guidelines" (MHRD guidelines dated 11/03/2016) may be referred.